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Radiation-Hard Step-up DC-DC Converter

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Abstract

DC-DC converters play an important role in electronic systems in all domains of application. In the consumer electronics market, which shows continuous growth, the need for lighter and more ergonomic devices has increased the demand for inductorless converters. Due to their smaller size and weight, switched-capacitor converters have grown in popularity. Since they can be designed exclusively with capacitors and switches, they can be fully integrated on-chip, which makes them suitable for mobile applications.

Nevertheless, portable or not, if an electronic device is subject to radiation it may fail due to functional errors and/or structural degradation. Devices with radiation hardening features find more applications in space and nuclear technology. At the Earth's surface level, electronic systems can be affected by radiations as well. And since the number of sensitive and critical devices has increased in the last decades, the need for radiation hardened electronics is more and more imperative in different areas of electronic devices applications.

This work addresses the study and design of a radiation hard step-up switched-capacitor DC-DC converter, designed with 0.35 μm CMOS technology, to be used in the readout electronics of the CERN's LHC experience. The functional specifications are: output of 2.5 V for an input of 1.2 $\pm$ 0.3 V and with a load current capability of 100 mA. A PWM control has been adopted to regulate the output voltage, employing a variable voltage sawtooth generator with a switching frequency of 10 MHz. Some functional considerations were used to ensure some radiation hardening features.

Keywords: CMOS, IC design, PWM control, radiation hardening, step-up DC-DC converter, switched-capacitor.

Acknowledgments

I would like to thank my supervisor, professor José Machado da Silva, for his guidance and wise advices. João Carvalho for his precious assistance. Marc Fernandes, for all his companionship. I am also grateful to my parents for all the unconditional support during, not only the development of this project, but all my life and for always encouraging my passion for science.

Helena Vargas

"All truths are easy to understand once they are discovered.
The point is to discover them."

Galileo Galilei

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Abbreviations and Symbols

List of Abbreviations

BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
EMI	Electromagnetic Interference
IC	Integrated Circuit
LHC	Large Hadron Collider
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	*n*-channel MOSFET
PWM	Pulse Width Modulation
PMOS	*p*-channel MOSFET
PSRR	Power Supply Rejection Ratio
RHBD	Radiation Hardening-By-Design
SCR	Silicon-Controlled Rectifier
SEB	Single-Event Burnout
SEE	Single-Event Effect
SEGR	Single-Event Gate Rupture
SEFI	Single-Event Functional Interrupts
SELU	Single-Event Latch-Up
SET	Single-Event Transient
SEU	Single-Event Upset
TID	Total Ionizing Dose

List of Symbols

B	body	-
$C_k\|_{k\in[1,n]}$	flying capacitors	(F)
C_L	load capacitor	(F)
C_{ox}	oxide capacitance per unit area	(F/m^2)
D	drain, duty-cycle	-, (%)
$d_{dt1,dt2}$	dead time between ϕ_1 and ϕ_2	(%)
$D_{\phi 1}$	odd switch duty-cycle	(%)
$D_{\phi 2}$	even switch duty-cycle	(%)
η	energy efficiency	(%)
f_s	switching frequency	(Hz)
f_{osc}	oscillator frequency	(Hz)

ϕ_1	stage 1 command signal	(V)
ϕ_2	stage 2 command signal	(V)
G	gate	-
i_d	drain current	(A)
I_o	DC load current	(A)
k_n	NMOS transconductance	(μA/V^2)
k_p	PMOS transconductance	(μA/V^2)
L	channel region length	(μm)
n	number of flying capacitors	-
N	number of oscillator inverters	-
P_i	input power	(W)
P_o	output power	(W)
$r_{on,n}$	type n MOSFET on-resistance	(Ω)
$r_{on,p}$	type p MOSFET on-resistance	(Ω)
r_{S1}	stage 1 switch on-resistance	(Ω)
r_{S2}	stage 2 switch on-resistance	(Ω)
R_L	load resistance	(Ω)
S	source	-
$S_{1,i}\|_{i\in[1;2n]}$	switches controlled by ϕ_1	-
$S_{2,j}\|_{j\in[1,n+1]}$	switches controlled by ϕ_2	-
t_o	operation time	(s)
t_{pHL}	propagation time from high to a low logic level	(s)
t_{pLH}	propagation time from low to a high logic level	(s)
t_{r1}, t_{r2}	relative time	(s)
T_s	switching period	(s)
W	channel region width	(μm)
$v_C(t)$	instantaneous flying capacitor voltage	(V)
$v_{control}(t)$	output voltage amplified error	(V)
Vdd	positive source voltage	(V)
v_{DS}	drain-source voltage	(V)
v_{GS}	gate-source voltage	(V)
$v_o(t)$	instantaneous output voltage	(V)
v_{SD}	source-drain voltage	(V)
v_{SG}	source-gate voltage	(V)
V_i	input voltage	(V)
V_o	DC output voltage	(V)
$V_{T,n}$	NMOS threshold voltage	(V)
$V_{T,p}$	PMOS threshold voltage	(V)
β_n	NMOS transistor gain	(μA/V^2)
β_p	PMOS transistor gain	(μA/V^2)
ΔV_o	output voltage ripple	(V)
λ_n	channel modulation effect in the NMOS	(V^{-1})
λ_p	channel modulation effect in the PMOS	(V^{-1})
μ_n	electron mobility in the n channel	$\frac{m^2}{V.s}$
μ_p	electron mobility in the p channel	$\frac{m^2}{V.s}$

Chapter 1

Introduction

Direct current to direct current (DC-DC) converters play an important role in current electronic systems. They serve as an interface between two DC power supplies, allowing the conversion of one voltage level to another, and control the power flow between them [8]. They are used in a large variety of power ranges and applications, such as CD players, cellphones, PC power supplies and hybrid or electric vehicles.

The main components present in a DC-DC converter are switches, inductors and capacitors. In DC-DC converters where inductors are used, these components are responsible for the transfer of energy between input and output. With a proper command, switches are turned on and off in order to charge or discharge the inductor, allowing the stepping up or down of the output voltage. The capacitor is placed in parallel with the output to provide energy storage and ensure a constant DC output voltage.

There are different topologies available, but the two most important ones are the step-up and the step-down converters, where the output voltage or current (relatively to the DC input) is stepped up or down, respectively. All other topologies, such as the buck-boost and Cúk converters, result from the combination of these two basic topologies [9].

According to the application and the magnitude of the step between the input and the output, it may be necessary to electrically isolate the converter. Isolated converters use a transformer to achieve the desired isolation. Unlike the non-isolated converters, there is no need to include an inductor involved in the energy transfer process, since this task is held by the transformer windings. Among the most commonly used isolated topologies are the flyback and forward converters.

The use of inductors implies an increase of converters' weight and volume and is responsible for a fair amount of electromagnetic interference (EMI) that can affect the proper functioning of the converter itself or of neighbour systems. So, in certain applications, the employment of these components is inconvenient. As an alternative, capacitors can be used in the energy transfer between input and output. A converter mainly composed by switches and capacitors is known as a switched-capacitor converter. Since this type of converters are inductorless, they occupy less space, are lighter and therefore are more suited for mobile applications and monolithic integration.

Design specifications strongly depend on the application. Not all converters are suited to

withstand harsh conditions, specially environments with high radiation. In these situations it is imperative to use special technologies and design techniques, called radiation hardening, with the purpose of improving the tolerance of converters' electronics to radiation. These converters find applications in space systems, such as satellites and space stations, or in nuclear reactors. That is the case also of the electronics used in the readout systems of the Large Hadron Collider (LHC) [10] at CERN.

The LHC is the world's most advanced particle physics instrument. In its facilities, placed about 100 m underground, sub atomic particles (the "Hadrons"- either protons or lead ions) travel in opposite ways inside a 27 km long circular accelerator speeding up each lap. When particles reach high state of energy they are brought into collision in four different experiments, each one installed in a large underground cavern. These experiments produce significant amounts of data that is later distributed by a grid computing system [11].

It is not only in these specific facilities or in outer space that radiation is a concern. On Earth's surface electronic devices also experience radiation effects and the resulting performance deviation is becoming an increasing problem due to modern societies dependence of sophisticated electronic systems that cannot fail or malfunction.

In DC-DC converters the effects of radiation are, for instance, responsible for a degradation of efficiency and output voltage quality. Special care has to be taken when choosing the semiconductors type, external capacitors dielectric material, layout techniques, shielding and eventually redundancy techniques, in order to improve radiation hardening characteristics.

1.1 Main goal and system requirements

The main goal of the dissertation is to study and design a radiation hardened switched capacitor DC-DC step-up converter using a 0.35 μm CMOS technology. The primary established system specifications are shown in table 1.1.

Table 1.1: System requirements.

	Value	**Unit**
V_o	2.5	V
V_i	1.2 ± 0.3	V
Vdd	3	V
I_o	100	mA
ΔV_o	1	%

V_o represents the desired DC output voltage and ΔV_o represents the maximum voltage ripple required. So, the instantaneous output voltage value can be $v_o(t) = 2.5 \pm 0.025$ V, but the steady state mean value needs to be $V_o = 2.5$ V. V_i symbolises the DC input voltage, with the respective tolerance. Vdd represents the positive DC source voltage and I_o represents the maximum required load current.

1.2 Document structure

In order to present the work developed, this document was divided as follows:

Chapter 2: Literature Review and State of the Art Summary of the preliminary research done on several topics, such as switched-capacitor converters (topologies and control), semiconductor physics, CMOS technology, radiation hardening and radiation hardened converters.

Chapter 3: Theoretical Analysis Theoretical study of the converter topology. Presentation of the theoretical model results. Calculation of some key parameters, such as maximum switch on-resistance and capacitance values. Theoretical analysis of the closed-loop regulation block

Chapter 4: Behavioural Simulations Presentation and results discussion of high level simulations performed to verify if the converter, as well as the regulation block, meet all the established requirements. Validation of the theoretical model deduced.

Chapter 5: Simulations With More Realistic Models Presentation of more realistic simulations, performed, using components design down to the transistor level, instead of employing functional models. Circuit description and results discussion.

Chapter 6: Conclusions and Future Work Discussion of overall results, list of difficulties encountered along the project and indication of possible improvements.

Appendixes A, B and C Auxiliary material such as simulation raw data, data processing and graphical plots, mathematical deductions and produced source code.

Chapter 2

Literature Review and State of the Art

2.1 Step-up DC-DC converter

The step-up converter, also known as the boost converter, is one of the DC-DC converters' basic topologies. As the name implies, the converter produces an output voltage higher than the input voltage. Since the input voltage required for the project is stepped up by a ratio of approximately 1:2 there is no need for electrical isolation, because the step ratio is small. Besides, one of the goals of the project is to design an integrated converter, and thus the reduction of the number of magnetic elements is an important factor. Hence, the theoretical study will only address non-isolated converters.

2.1.1 Classic topology

The basic step-up converter is shown in figure 2.1.

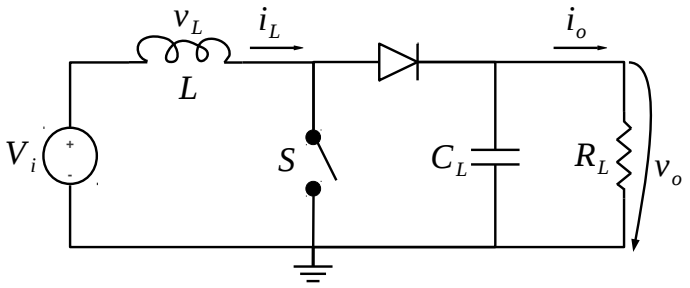

Figure 2.1: Basic DC-DC Step-up Converter.

Its operation is the following: when the switch is on, the diode is reverse biased and the current only flows through the inductor, charging it with electromagnetic energy. During this period, while the output is disconnected from the input (figure 2.2(a)), the capacitor supplies energy to the output. On the other hand, when the switch is off, there ir current flowing in all circuit branches, and the load is supplied with energy from both the input and the inductor (figure 2.2(b)).

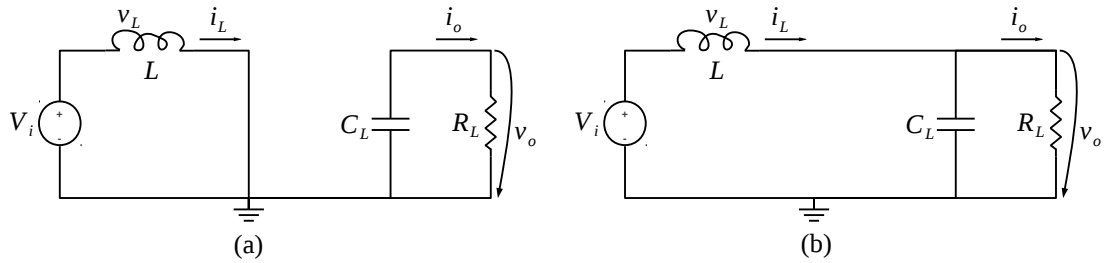

Figure 2.2: Step-up Converter: (a) Switch on; (b) Switch off.

The process described above represents the basic principle of operation of the step-up converter. However, to obtain the desired voltage level at the output, it is necessary to properly regulate the energy stored in the inductor and consequently transferred to the output. So, the duty-cycle (D) of the control wave of the switch is a fundamental parameter. The ideal relationship between the steady state value of the output voltage, the switch duty-cycle and the input voltage is given by equation 2.1.

$$\frac{V_o}{V_i} = \frac{1}{1-D} = M(D) \tag{2.1}$$

where M(D) is the voltage conversion ratio of the converter.

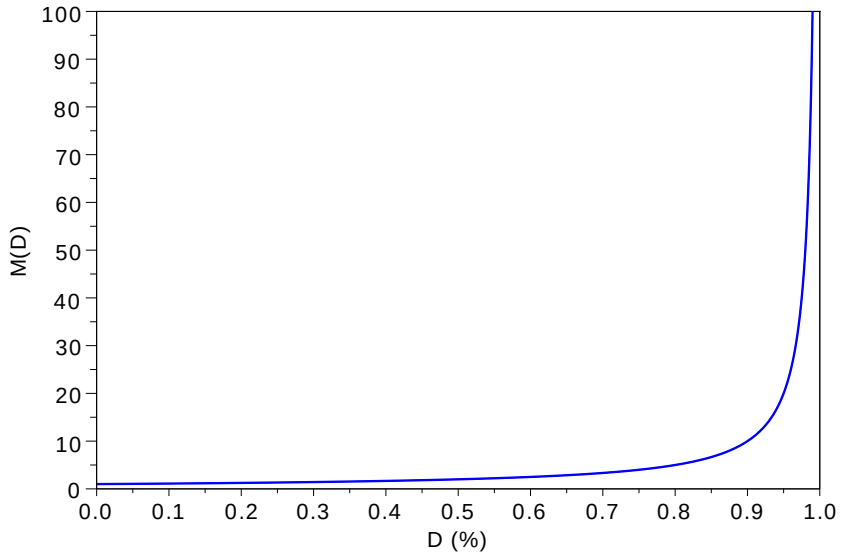

Figure 2.3: Step-up converter ideal voltage ratio.

Equation's 2.1 plot is shown in figure 2.3. From this figure it can be seen that, ideally, the conversion ratio is infinite when the duty-cycle is 1, but in practice, due to the non-ideal characteristics of the circuit components, there is a limit for the output voltage. The relationship given by equation 2.1 yields when the converter operates in the continuous conduction mode, which

means that the inductor does not fully discharge and the current never reaches zero. If the inductor current reaches zero and the converter enters the discontinuous conduction mode, some properties of the converter suffer considerable changes. For instance, the voltage conversion ratio becomes load dependent and therefore the output voltage ceases to be only a function of the duty-cycle and the input voltage. This conduction mode frequently occurs in converter operating at light loads or with no load at all.

Despite of widely used and well covered in the literature, inductor converters have a certain number of disadvantages and are not suited for certain of applications. For instance, applications where the size and weight are important factors or EMI shielding is difficult, such as mobile devices, power supplies, battery charging systems. A step-up converter needs a storage element to elevate the output voltage. That function, as it was previously described, is normally accomplished by employing an inductor. However, the inductor is usually a very large element, compared to the rest of the circuit, and increases significantly the size and weight of the converter and in general is not implementable on chip. Besides, large inductors have large parasitic resistances, which increases the power losses of the circuit and lowers the converter overall efficiency. One way of overcoming the oversized inductor issue is increasing the switching frequency. But as a consequence, high switching frequencies generate electromagnetic interferences which can disrupt the proper operation of the converter. Some technologies that allow the implementation of relatively small size inductors on-chip have been developed. These technologies make more feasible the converters' design that require more than one inductor. Figure 2.4 shows a step-up converter with two inductors and figure 2.5 shows the respective on-chip application.

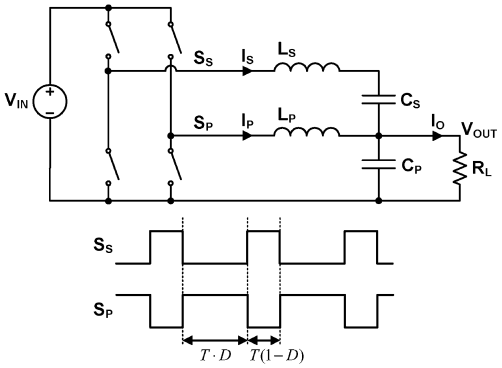

Figure 2.4: Stacked interleaved topology and timing diagram [1].

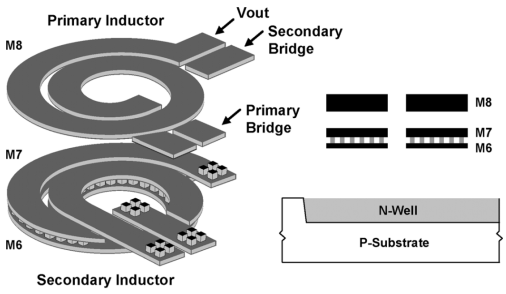

Figure 2.5: On-chip coupled inductor realization [1].

However, despite the advancements on inductors on-chip integration, these circuit elements are still very large and, as it will be seen in section 2.4.1, reducing the size of the converter is an important matter. After some research, an alternative to the conventional inductor converter was found - the switched-capacitor based converters.

2.1.2 Switched-capacitor DC-DC converters

Switched-capacitor DC-DC converters in general use only switches and capacitors to achieve the desired voltage conversion. For this reason, they are more suitable for integration than the conventional converters made with magnetic elements. For many years, the employment of this type of converters has been restricted to simple applications, normally requiring fixed integer voltage conversion ratios. In fact, the switched-capacitor converters domain is still in development. There are several published papers dedicated to the analysis of different topologies, but despite the several analysis available, some of the existing ones do not converge and sometimes it seems there exists some misconceptions around the subject. Also, there are some issues related with the regulation of these converters that have been the focus of researchers, at least in the past two decades. However, in the last years, due to technological advancements in the control and chip manufacturing areas and due to the increasing number of studies around the subject, more and more of these converters are appearing in the market.

One of the early publications[12] was from J.F. Dickson and introduced what became later known as the Dickson topology. Since then, several new topologies or improved variants of the existing ones have been introduced and analysed by different authors. The five most notorious switched-capacitor DC-DC step-up converters are the Ladder, Dickson, Fibonacci, Series-Parallel and the Doubler topologies. The basic schematics for two clock signals are shown in figure 2.6.

Ideally, the voltage conversion ratio of a typical switched-capacitor DC-DC boost converter is $n+1$, where n, represents the number of flying capacitors in the circuit. The flying capacitors are the capacitors whose configuration is "rearranged" in the circuit by the switching process in order to provide the energy transference operation. In figure 2.6 they correspond to capacitors C_1, C_2 and C_3. Meaning that theoretically, the output voltage can be stepped $n+1=4$ times. The schematics shown here represent two stage converters since their switches can be controlled with two main clock signals: ϕ_1 and ϕ_2, dividing the converter operation into two main operating stages: charging the flying capacitors and then discharging the stored energy in order to step up the output voltage. But, if the same circuit is expanded or combined with other topologies and controlled with N clock signals, ϕ_1 through ϕ_N, a multi-stage converter can be created with an expanded conversion ratio range.

Contrary to the inductor-based converters, where the conversion ratio is ideally defined by the duty-cycle, traditionally, switched-capacitor converters have a fixed voltage conversion ratio. During many years, the control of the switched-capacitor converters was made in open-loop. The flying capacitors were fully charged, normally with a duty-cycle of 50 % and then discharged. This method only allows a fixed voltage step and then makes the output highly dependent of the input voltage. With closed-loop regulation the flying capacitors are partially charged and never fully charged to the voltage level applied. The nominal charging operating point has to be in the middle of the linear part of the time charging characteristic of the capacitors. This allows enough manoeuvrability around the operating point, hence, to decrease or increase the capacitor charging time in order to regulate the output voltage in the event of line or load variations. However, by only

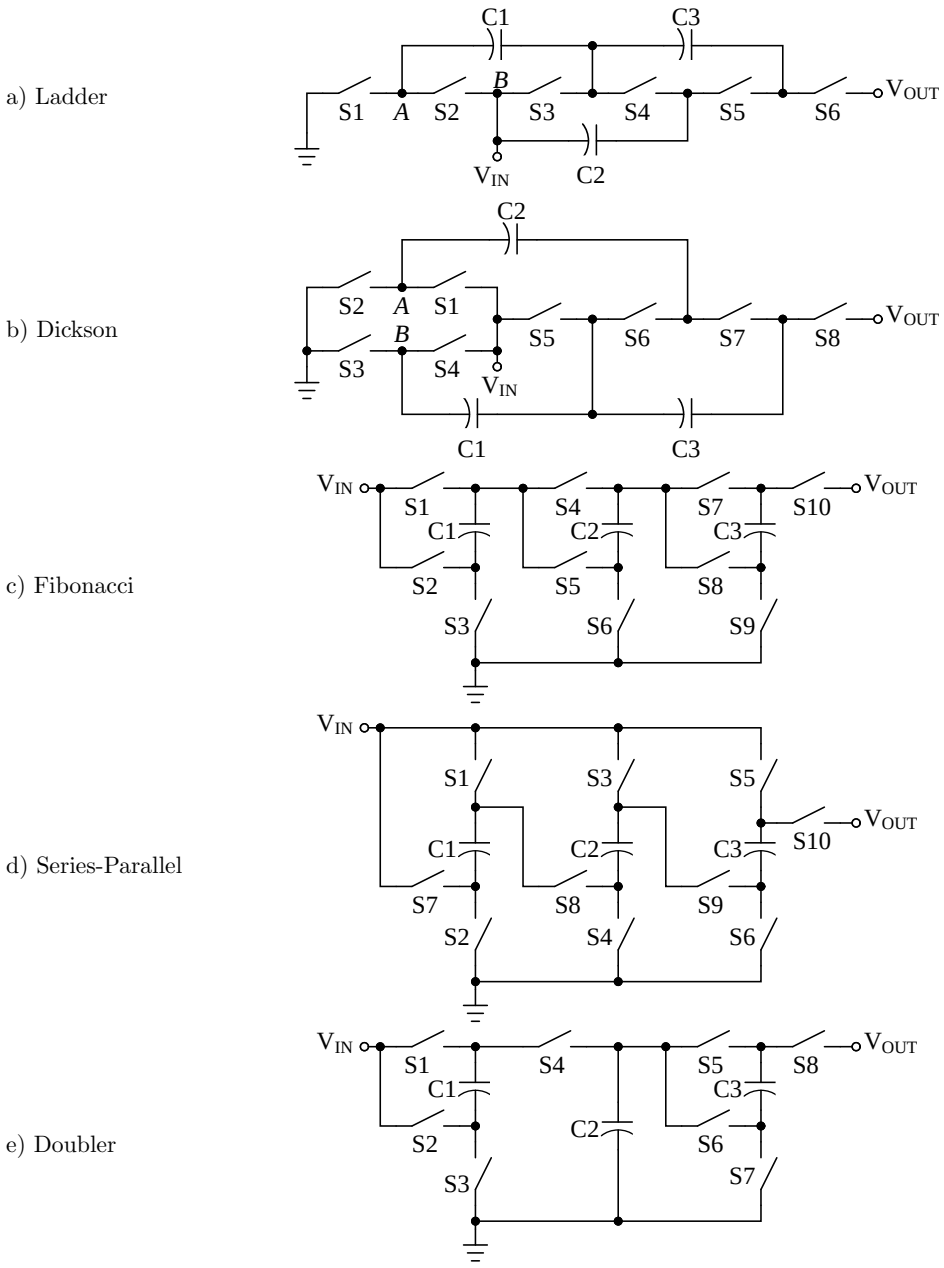

Figure 2.6: Five most notorious switched-capacitor DC-DC boost converter topologies [2].

charging partially the capacitors, the efficiency is lowered. So, a compromise between efficiency and line and load regulation has to be found. For any switched-capacitor converter, the primary issue is how to carry out the regulation requirement, which, as it was pointed out before, has been the subject of research at least in the past two decades [13].

To control the output voltage of a switched-capacitor converter three main variables can be manipulated: the switching frequency, the switches' duty-cycle operation and the switch conductance. Obtaining good transient and steady state responses with varying load and line conditions may be difficult. Since the load range of a switched-capacitor converter frequently changes dur-

ing operation, and the output voltage in most applications must be kept constant, among the three listed control variables, the switching frequency can be manipulated, but non-linear dynamics are associated with this type of control which can be difficult to model [2].

The output can also be regulated by manipulating the switch duty-cycle. Normally this is achieved by using pulse-width modulation (PWM) methods, where a control signal with a constant frequency is generated, but the pulse duration is variable. The implementation of PWM control methods can be simpler and more inexpensive then other control methods. However, converters regulated with classic PWM control are tuned to function around a certain operating point. In the presence of line and load variations, the DC output voltage and/or ripple value may deviate from the desired values, making the control a real challenge.

Sophisticated digital control or intelligent control methods were occasionally cited by some authors, for instance [14]. Yet, converters regulated with digital circuits, are more easily found, specially with a control based in state machines [15, 16]. The majority of solutions found for the closed-loop regulation were the classic PWM control or some optimized versions designed for the specific applications [14, 17, 18, 19, 20]. A common version found is a hybrid solution where the number of flying capacitors being charged and/or discharged is not static, but changes accordingly to the output requirements, varying the amount of charge being transferred. The output is then further regulated with a PWM control.

In the consulted literature, in most cases, an explanation why a PWM control was employed was not given. Since the regulation of these type of converters is such a concern, the most logic approach would be to employ more often some kind of intelligent control to obtain a more precise output regulation in the presence of load and line variations. However, that is not the case. Mainly because intelligent controllers normally require a processing unit (being a microprocessor or a relatively complex digital circuit), which raises the cost, complexity of the system, and increases the implementation area. Nevertheless, one of the main goals when adopting switched-capacitors converters is to replace the conventional inductor-based converters, and most of them are efficiently regulated with some form of PWM control.

2.2 Semiconductors

In order for an electronic device properly operate, the ability to control the flow of charged particles is essential. This ability can be achieved by semiconductors which can be manipulated to have a behaviour very similar to an insulator or a conductor when needed. For many decades, the predominant semiconductors used to manufacture electrical components were germanium and gallium. Nowadays, silicon is the most popular choice.

A silicon unit cell has a crystalline structure with a form of a tetrahedron with an atom at each vertex like the one shown on figure 2.7. But, for simplicity, the unit cell is often represented in 2D, as shown in figure 2.8.

A silicon atom has a core charge of +4 and has a total of 14 electrons, 4 of which are valence electrons that bind the atoms together.

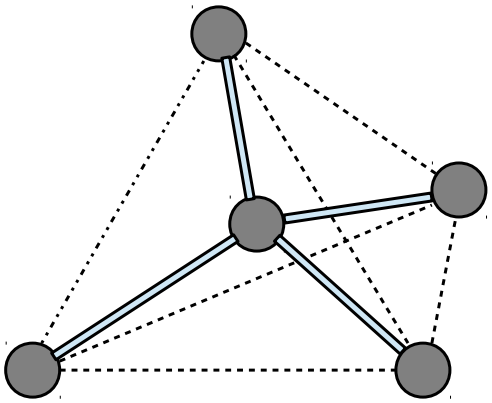

Figure 2.7: Silicon single-crystal structure (3D).

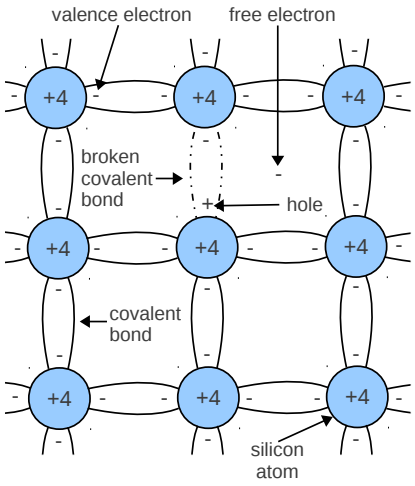

Figure 2.8: Silicon crystal structure (2D): Intrinsic semiconductor (based on [3]).

When the semiconductor is subjected to certain temperatures, the covalent bonds are broken and the electrons are freed. The absence of the electron in the covalent bond is called a hole. When holes are formed, the electrons in the neighbouring atoms can leave their covalent bonds and fill the holes left by other electrons, and consequently, the new hole left by that electron can be filled by another neighbouring electron. Thus, from an outside observer perspective, it is given the impression that the holes themselves are moving and not the the electrons. This hole motion can be random or controlled if an electromagnetic field is applied. This way, it is possible to control the flow of charged particles, producing electric current.

If the crystal structure is a pure sample of silicon and has no foreign atoms, it is called an intrinsic semiconductor. Consequently, the hole concentration p and the electron concentration n must be equal and the intrinsic concentration n_i, which is temperature-dependent, is given by $n_i = p = n$.

When the crystal has impurities in its structure, the semiconductor is called extrinsic or doped. The addition of impurities is a common practice used to increase the number of carriers. The number of carriers defines if the semiconductor is an n-type or a p-type one. Most physical and chemical properties are very similar to those of the intrinsic silicon crystal, only the electrical properties change.

When an intrinsic semiconductor is doped with pentavalent impurities (called donors), such as antimony, phosphorus or arsenic, the number of electrons increases and the number of holes decreases. Consequently, the dominant carriers are the negative electrons witch results in an n-type semiconductor. On the other hand, when an intrinsic semiconductor is doped with trivalent impurities (called acceptors), such as boron, gallium or indium, the dominant carriers become the holes and this type of crystal is called p-type semiconductor [21].

2.2.1 The pn junction

Combining *n*-type and *p*-type silicon layers in different ways, several semiconductor devices can be produced. Each combination leads to unique electrical characteristics. Examples of commonly used semiconductor devices are the diode, the bipolar transistor (BJT), the thyristor and the metal–oxide–semiconductor field-effect transistor (MOSFET). In the next subsections devices based on the MOSFET will be studied, since the main goal is to design an on-chip complementary metal-oxide semiconductor (CMOS) converter and all the components will have to be implemented with metal–oxide–semiconductor (MOS) technology.

2.2.2 The MOSFET

The MOSFET is named after its unique physical structure. The concept of field effect transistor was patented by J. E. Lilienfeld in the beginning of the 1930s, before the invention of the bipolar transistor. However, due to manufacturing limitations these technologies only became practical in the early 1960s [22]. Over the years, technological advances made the MOSFET one of the most employed semiconductor devices in both digital and analogue circuits. It is simpler to manufacture than a bipolar transistor, occupies smaller on-chip space, can be connected as resistor, a capacitor or a diode, which makes possible the design of systems consisting exclusivity of MOSFETs [21].

There are two types of MOSFET: The *n*-channel MOSFET or NMOS transistor and the *p*-channel MOSFET or the PMOS transistor. Their operation is very similar, but there are some structural and electrical differences.

In essence, the MOSFET is a four terminal device. The corresponding circuit symbols for the NMOS and PMOS used in this work are shown in figures 2.9 and 2.10.

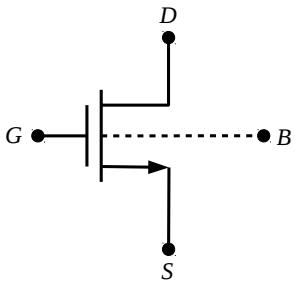

Figure 2.9: NMOS four terminal symbol.

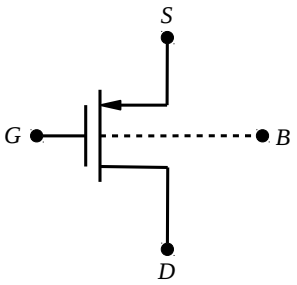

Figure 2.10: PMOS four terminal symbol.

The terminal names are drain (D), source (S), gate (G) and body (B). The body terminal is connected with a dashed line, since it is often not represented, making the MOSFET a three terminal device. When that is the case, it is assumed that the body terminal is connected to the ground (gnd), in the case of the NMOS transistors, or to the positive supply voltage source (vdd), in the case of the PMOS transistors. This way, the drain-source current becomes only dependent of the gate-source voltage applied.

The NMOS body is made of p-type silicon and the source and drain are made of heavily doped (n^+) silicon layers, which are inserted in the body layer. The PMOS body is made of n-type silicon and the source and drain are made of heavily doped (p^+) silicon layers. In both type of transistors, a silicon oxide (SiO_2) layer covers a portion of the surface of the source, drain and body regions. The gate terminal consists of a metal electrode placed above the oxide region, making the gate electrically isolated from the body. The source and drain terminals are also made of metal electrodes, but directly attached to the semiconductor material. The physical structure of the NMOS transistor can be seen in more detail in figure 2.11.

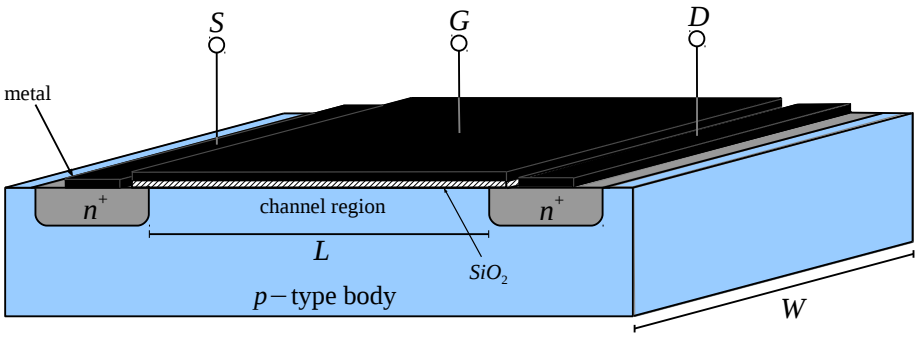

Figure 2.11: NMOS physical structure.

The letters L and W refer to the channel region length and width. From this figure it is visible that there are two pn junctions between the source and drain, which means that when no gate voltage is applied, two back-to-back diodes exist between these to regions and no current flows between them. When a source-voltage is applied, the MOSFET can operate in three distinct regions: cut-off, triode and saturation regions. In triode and saturation regions, an n-type or a p-type conduction channel is formed, if an NMOS or a PMOS respectively, in the channel region, allowing the flow of electric current between the source and drain terminals. The drain current, drain-source and gate-source voltage equations of each region are given in table 2.1.

Table 2.1: Main equations of the NMOS and PMOS transistors in each operation region.

	NMOS			PMOS		
	v_{DS}	i_D	v_{GS}	v_{SD}	i_D	v_{SG}
cut-off	---	0	$<V_{T,n}$	---	0	$<\lvert V_{T,p}\rvert$
triode	$<v_{GS}-V_{T,n}$	$\beta_n\left[(v_{GS}-V_{T,n})v_{DS}-\frac{v_{DS}^2}{2}\right]$ for $v_{DS}\ll 2(v_{GS}-V_{T,n})$ $\Rightarrow\beta_n(v_{GS}-V_{T,n})v_{DS}$	$\geq V_{T,n}$	$<v_{SG}-\lvert V_{T,p}\rvert$	$\beta_p\left[(v_{SG}-\lvert V_{T,p}\rvert)v_{SD}-\frac{v_{SD}^2}{2}\right]$ for $v_{SD}\ll 2(v_{SG}-\lvert V_{T,p}\rvert)$ $\Rightarrow\beta_p(v_{SG}-\lvert V_{T,p}\rvert)v_{SD}$	$\geq\lvert V_{T,p}\rvert$
saturation	$\geq v_{GS}-V_{T,n}$	$\frac{1}{2}\beta_n(v_{GS}-V_{T,n})^2(1+\lambda_n v_{DS})$ for $\lambda_n v_{DS}\ll 1$ $\Rightarrow\frac{1}{2}\beta_n(v_{GS}-V_{T,n})^2$		$\geq v_{SG}-\lvert V_{T,p}\rvert$	$\frac{1}{2}\beta_p(v_{SG}-\lvert V_{T,p}\rvert)^2(1+\lambda_p v_{SD})$ for $\lambda_p v_{SD}\ll 1$ $\Rightarrow\frac{1}{2}\beta_p(v_{SG}-\lvert V_{T,p}\rvert)^2$	

$V_{T,n}$ and $V_{T,p}$ represent the threshold voltage, λ_n and λ_p, with units V^{-1}, characterize the channel modulation effect in NMOS and PMOS respectively. All parameters are dependent of the manufacturing technology.

Together, the gate metal plate and the channel region are equivalent to a parallel plate capacitor where the dielectric is the silicon dioxide layer and the capacitance per unit area is represented by C_{ox}. Considering μ_n and μ_p as the electron mobility in the channel, also a value dependent of the manufacturing technology, the NMOS and PMOS transconductance with units A/V^2 is defined as $k_{n,p} = \mu_{n,p} C_{ox}$.

The gains β_n and β_p present in the drain current equations is given by

$$\beta_n = k_n \frac{W}{L} \tag{2.2}$$

$$\beta_p = k_p \frac{W}{L} \tag{2.3}$$

If v_{DS} is kept small enough, in the triode region, for a constant drain-source voltage, the on-resistance of the MOSFET is given by

$$r_{on,n} = \frac{1}{\beta_n (V_{GS} - V_{T,n})} \tag{2.4}$$

$$r_{on,p} = \frac{1}{\beta_p (|V_{GS}| - |V_{T,p}|)} \tag{2.5}$$

Equations 2.2 to 2.5 are very important for the MOSFET design as a switch, as well as the equations of table 2.1 relative to the triode region. However it is important to point out that the models and subsequent equations indicated so far are more suited to describe long channel MOSFETs. For short channel transistors, the models are far more complex, and find applications only in computation analysis. For a quick analysis and a few "hand" calculations, the equations presented are a reasonable approximation.

2.2.2.1 High gate-source voltage requirements

For the transistor to operate in the triode region, some conditions have to be met, as shown in table 2.1. Due to voltage drops in the circuit in which the MOSFET is placed, despite of the gate voltage applied, sometimes it is difficult to ensure that the triode region conditions are met, and the MOSFET may not function as a switch, as expected. This issue is common in some switched-capacitor converter topologies. To circumvent this problem, external circuits, such as level shifters and bootstrapping circuits can be employed to generate the higher voltage clock signals, but these solutions increase the silicon implementation area, as well as the converter's design complexity. A more simple solution, shown in figure 2.12, was proposed by [4].

Inside the switch cell, the PMOS M_c acts as a switch. It is driven by the boosting NMOS M_a and PMOS M_b. To turn the switch M_c on, a high clock signal is applied to M_a and 0 V appears at

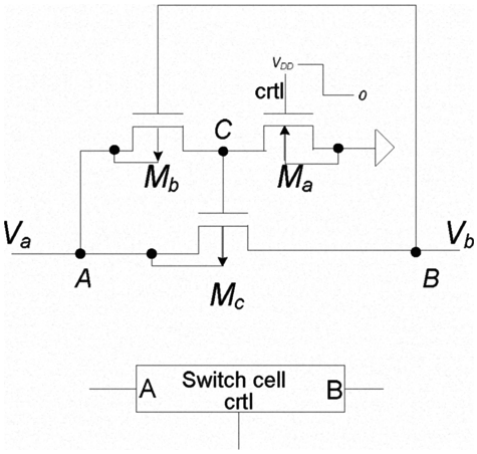

Figure 2.12: Switch with constant ON V_{GS} mechanism [4].

node C, passing V_a to node B, with a certain voltage drop. M_b will then turn off due to the higher voltage in node B, connecting its gate and source to nodes B and A, respectively. When a low clock signal is applied, M_a shuts down. Now node B has a lower voltage then node A and M_b will turn on passing V_a to node C, turning M_c off.

M_a has to be designed with a large aspect ratio to increase the overdrive voltage of M_c. M_b has to be designed with a small aspect ratio to limit the leakage current. This way, M_b can be closed faster being node B voltage updated at a faster rate. This solution allows switch M_c to be turned on and off completely by applying a clock signal varying from 0 V to Vdd only, without relying on the node voltages of the circuit itself.

2.3 CMOS technology and the IC design

When choosing if an application is going to be implemented by an integrated circuit or a discrete version, the answer may not be always clear. It is not set in stone if one is better than the other, as it really depends on the application, main objectives and costs involved. But in general, an integrated circuit, in comparison with its discrete counterpart, may present better speed and accuracy, the implementation area is smaller and its mass production is less expensive.

A single chip can contain over a billion transistors, and the amount of transistors that can "fit" in a chip is increasing every year. So, there are some applications that can only be achieved by integrated circuits and could never be achieved with discrete implementations.

CMOS technology employs both NMOS and PMOS transistors on the same chip, which has a number of advantages. A given CMOS process is defined by the minimum MOSFET channel length. For instance, for a 0.35 μm CMOS technology, all MOSFETs designed have a $L_{min} \geq 0.35$ μm. Due to technological advancements, the popularity of CMOS technology has grown over the decades. Compared with other types of transistors, the MOSFETs can be scaled down more

easily and the gate has a lower power consumption. Its operation can be manipulated in order to mimic other components behaviour like capacitors, resistors, and diodes, which allows the design of complete circuits entirely on-chip. The integrated capacitors have a capacitance of typically tens of pico Farads as the maximum capacitance density is relatively small. Maximum values of 1 $\frac{\mu F}{mm^2}$ are attainable today [23].

Thus, larger capacitors have to be implemented off-chip. However, the number of external capacitors, as well as external components should be reduced to a minimum, in order to minimize the number of chip pins. With CMOS, it is also possible to place both analogue and digital circuits in a single chip, reducing the packing cost and increasing the overall performance.

CMOS integrated circuit (IC) design is a very thorough and systematic process. It begins with the definition of circuit specifications, followed bt the selection of circuit topology and then comes the calculation of building component values and other important circuit parameters. After the layout of the circuit schematics, the next step is the simulation of the system. If the results are not the expected ones, then the process is restarted.

A schematic representation of the CMOS circuit design flow is shown in figure 2.13. The circuit specifications can change as the project matures. This is a critical process that should be carried out with models as realistic as possible. After the chip has gone to production, only some functional deviations may be corrected in case proper calibration circuits have been provided. In that sense, it is very important to understand the parasitics (capacitances, inductances and active devices) involved in the layout. A fundamental understanding of these problems is critical when very tight or extreme specifications are required for the design [5].

2.3.1 CMOS 0.35 μm process parameters extraction

It was seen in section 2.2.2 that the technological dependent parameters of the MOSFET model are k_n, $V_{T,n}$, k_p and $V_{T,p}$ which represent the transconductance and the threshold voltage of the NMOS and PMOS transistors, respectively. In order to extract the necessary process parameters of the 0.35 μm CMOS technology, several simulations were performed using Cadence® Virtuoso® Analog Design Environment.

The simulations performed were based on the circuit schematics shown in figures 2.14 and 2.15, where the main goal was to determine the steady state value of the gate-source voltage (V_{GS}) for a given DC drain current (I_D), in order to determine k_n, $V_{T,n}$, k_p and $V_{T,p}$.

In the schematics the gate terminal is connected to the source, connecting the MOSFETs as a diode, in order to minimize the effect of the channel modulation in the drain current. Through a series of tests it was concluded that the values of V_{DS} and V_{SD} did not significantly influence the V_{GS}-I_D relationship. So, for convenience, they were set to $V_{DS} = V_{SD} = 1$ V.

Two different scenarios were simulated:

Converter MOSFET design: In this scenario larger currents and transistor dimensions were considered, due to the specific project requirements. For each W={ 1000, 2000, 3000, 4000, 5000, 6000, 7000, 8000, 9000, 10000 } μm, the current I_D was defined with a sweep range of

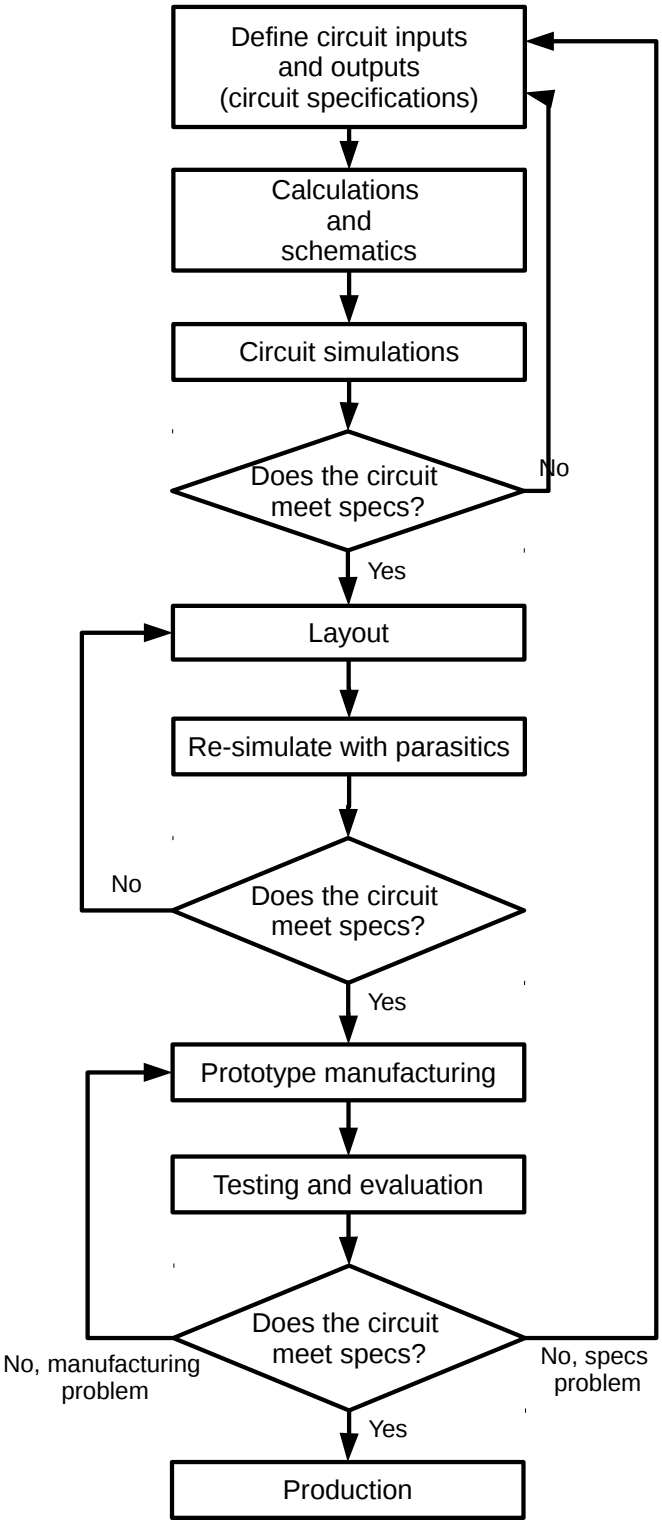

Figure 2.13: CMOS IC design process (based on [5]).

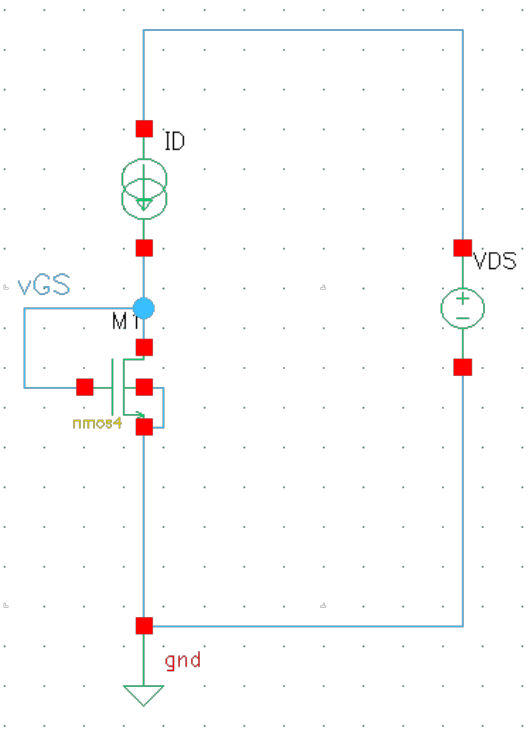

Figure 2.14: Circuit schematic used to determine the V_{GS}-I_D relationship for a given W for the NMOS transistor in order to determine the process parameters k_n and $V_{T,n}$.

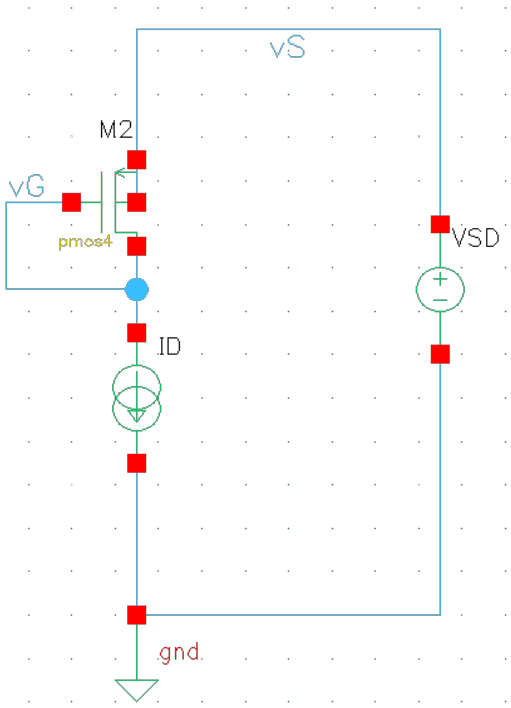

Figure 2.15: Circuit schematic used to determine the V_{GS}-I_D relationship for a given W for the PMOS transistor in order to determine the process parameters k_p and $V_{T,p}$.

[0;2] A. This interval was chosen accordingly to the maximum desired peak currents. The software stipulates a maximum of 10000 μm and for lower values than 1000 μm the resulting values of v_{GS} where very high and unpractical, which shows that for this current range, the MOSFETs need to have larger dimensions. The results of the DC analysis and the necessary follow up calculations are depicted in appendix A. With the results shown in tables A.9, A.10, A.13 and A.14, the values of k_n, k_p, $V_{T,n}$ and $V_{T,p}$ were plotted, respectively. Since for several W values, the process parameters did not converge to a specific value, hence it was necessary to use an iterative process to more accurately design each MOSFET present in the converter. The curves obtained are presented in appendix A in figures A.1 to A.4.

Regulation block MOSFET design: In this case smaller currents and transistor dimensions, were considered since in the control loop and other control sections of the circuit, the current magnitudes are smaller than the nominal current of the converter. For each W={ 5, 10, 20, 50, 100, 200, 500 } μm, the current I_D was defined with a sweep range of [0;1.5] mA. The results of the DC analysis and the necessary follow up calculations are depicted in appendix A. With the results shown in tables A.11, A.12, A.15 and A.16 the values of k_n, k_p, $V_{T,n}$ and $V_{T,p}$ were plotted, respectively. The curves obtained are shown in figures 2.16 to 2.19.

The process parameter values are not exactly the same for all W values, but in order to simplify

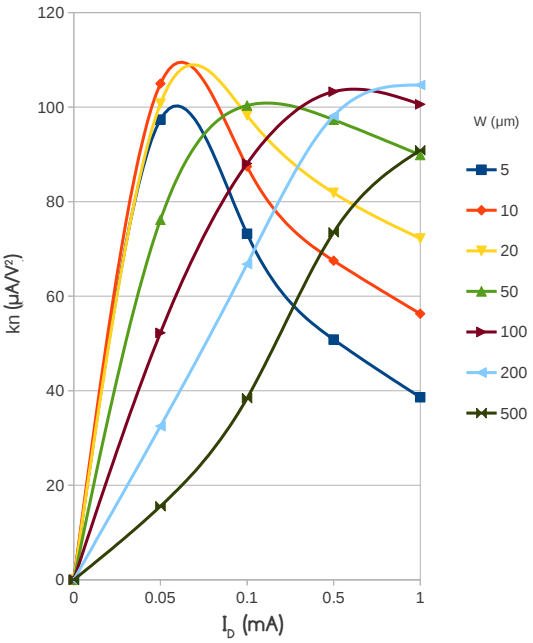

Figure 2.16: CMOS 0.35 μm process parameters: k_n vs I_D.

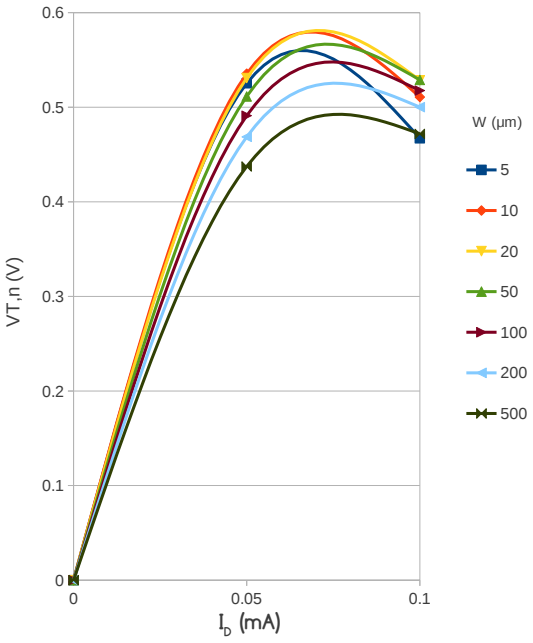

Figure 2.17: CMOS 0.35 μm process parameters: $V_{T,n}$ vs I_D.

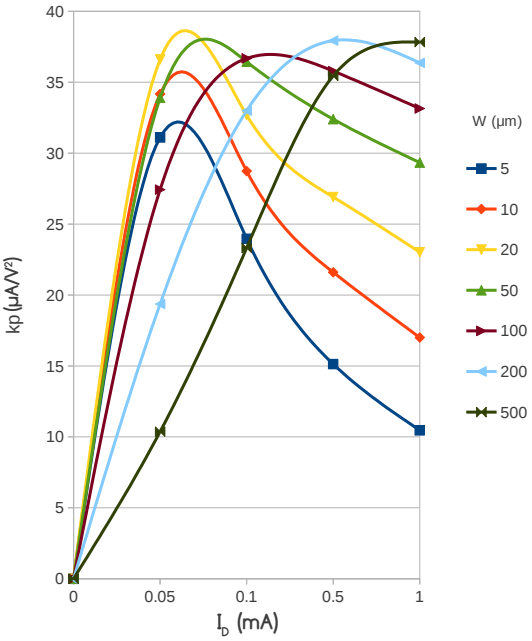

Figure 2.18: CMOS 0.35 μm process parameters: k_p vs I_D.

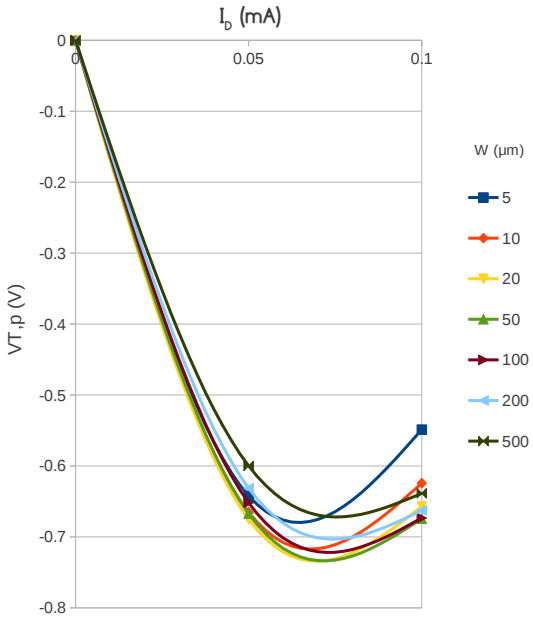

Figure 2.19: CMOS 0.35 μm process parameters: $V_{T,n}$ vs I_D.

the calculations, it was assumed that in these conditions the process parameters converge to certain values, which are indicated in table 2.2. These constants were used to design all the MOSFETs, except the ones acting as main switches in the converter.

Table 2.2: CMOS 0.35 μm process parameters used to design smaller and low current MOSFETs.

Parameter	Value	Units
k_n	100	$\mu A/V^2$
$V_{T,n}$	0.55	V
k_p	35	$\mu A/V^2$
$V_{T,p}$	-0.7	V

2.4 Radiation effects

2.4.1 Radiation hardening

When ionizing radiation hits an electronic device, its behaviour may change temporarily or permanently. These deviations may lead to small errors, such as a bit change in a digital circuit, or a catastrophic failure. The effects depend on the device type and robustness, pulse duration and intensity.

Radiation hardening techniques have been employed since the beginning of space exploration and have been perfected since then, alongside with the knowledge accumulated in the field of radiation and its effects. Nuclear power plants, particle accelerators, nuclear medicine equipments also need radiation hardened electronic equipment, since the employment of reliable electronic devices is crucial and the frequent replacement of parts due to radiation damage is not viable or affordable.

However, radiation effects are not present only in this type of specialised facilities or in outer space. On Earth's surface, electronic devices are also affected by radiation, but the effects are not as severe or as intense. With the rising number of solid state electronic devices and the increasing electronic systems' dependency of modern societies, these effects still can lead to critical safety situations, as it is the case with malfunctioning automotive electronics, medical equipment, cities pumping water systems or air traffic control, among others. The use of radiation hardened technologies have thus become more common.

2.4.1.1 Total ionizing dose effects

Incident radiation excites electrons in the valence band, creating electron-hole pairs. In the presence of an electric field, the electrons are readily swept away because their mobility in silicon is greater than the hole mobility. Thus, these charges drift in the material until they are recombined or trapped. In the gate oxide layer of MOS devices, the electron-hole pairs are rapidly separated when an electric field is applied. The electrons quickly drift away, while the slower holes became trapped, as they flow by, in the crystalline gaps of the oxide structure. The interface between the channel and oxide region also constitutes a trap site for holes. These traps induce a charge build up that changes the behaviour of the MOS device.

Trapped charges may shift the threshold voltages of MOS devices. In digital electronic circuits this originates high leakage currents and affect the device operation timing. It either may result

in a deficient control or total inability to shut-off the source-drain current and increase the device power consumption. Linear electronic circuits can also be affected since input bias current, offset, and drift as well as voltage offset and drift will change. Bias and quiescent currents equally increase over time [6]. This phenomenon is known as total ionizing dose (TID) and its effects are cumulative and normally become more evident with time.

2.4.1.2 Displacement damage

If enough energy is transferred to an atom, it can be freed from its lattice site to an interstitial site, creating a shallow level trap in the material. Deep level traps can act as generation, recombination or trapping centres which can decrease the minority carriers lifetime, increase the thermal generation rate of electron-hole pairs and reduce the mobility of carriers. Displacement damage is a concern primarily for minority carriers, such as bipolar transistors, and optoelectronic devices. It has little importance in MOS devices [24]. Similarly to TID, displacement damage is cumulative and its effects normally become more evident over time.

2.4.1.3 Single event effects

A single-event effect (SEE) can be generated trough several mechanisms, but usually occurs when a charged particle travels through the device and ionizes the device material, losing energy in the process. SEE can be destructive, resulting in catastrophic device failure, or non-destructive, resulting in data loss and/or device control loss [6].

The errors caused by SEE can be classified as soft or hard errors. A soft error is not destructive and can be corrected by reprogramming the circuit, resetting it into its correct logic state or by restarting an algorithm. Hard errors cannot be corrected by reprogramming and can cause physical damage in the circuit [24].

SEE can have repercussions in long term, but usually its effects are sensed right way. The most common SEE are the following [6]:

Single-Event Upset Single-Event Upsets (SEU) occur when a high-energy heavy ion strikes a circuit, changing the state of a bistable element, such as a flip-flop or a memory cell, causing false information to be stored. SEU effects are non-destructive and cause soft errors, since the situation can be reverted by rewriting the effected element.

Single-Event Transients Single-event transients (SET) are caused by a nearby passage of a charged particle that may momentarily change the voltage drop in a circuit node, causing a current transient in a integrated circuit. SET do not physically damage the circuit, but can corrupt data. Since they are often of a transient nature, they can just be handled as a noise source during data processing.

Single-Event Functional Interrupt Single-event functional interrupts (SEFI) are usually caused by a particle strike. The effects are not destructive but can produce data, control or functional-interrupt errors that require complex or extreme recovery actions, such as system wide reboot.

Single-Event Latch-Up In 4-layer structures, such as CMOS ICs, a parasitic element commonly known as a silicon-controlled rectifier (SRC) is present. Due to a single-particle energy deposition in the base region, the current flowing in this element may become very large. This phenomenon induced by a single charged particle is referred as a single-event latch-up (SELU). This event can cause permanent damage to the device or IC.

Single-Event Burnout and Single-Event Gate Rupture Single-event burnout (SEB) and single-event gate rupture (SEGR) are more concerning in power devices. In SEB a charged particle strike may induce high current flow in the parasitic *npn* bipolar structure of the vertical power MOSFETs, with the risk of permanently damaging the device. SEGR occur when incident particles produce charge build up in the gate dielectric around the gate of a power MOSFET, forming a conduction path in the gate oxide. Both SEB and SEGR originate hard errors since they cannot be corrected by reprogramming and have physically damaging consequences, sometimes on a catastrophic level.

2.4.2 Radiation hardening techniques

Radiation hardening by design (RHBD) has grown in popularity among designers over the years. The techniques that can be employed to mitigate radiation effects are the following:

Shielding One way of protecting the circuit from ionizing radiation is by enclosing it, or sections of it, in tantalum or tungsten. However, shielding increases the weight of the device. The reduction of electron impact on low-energy proton dose is very effective, but the rate of SEEs caused by high-energy cosmic rays is not reduced. Moreover, thick shielding can increase the SEE rate, due to the creation of multiple secondary particles which are a result of the interactions between the cosmic rays and the shield material [6].

Derating System operation (or only some system components) below the nominal point of operation. During irradiation, if some parameters change, such as current magnitude or voltage swings, the system may still function within normal standards.

Redundancy The system, or sections of the system, are replicated and function in parallel. If one element fails, the others ensure the continuous operation. Usually there is some kind of voting mechanism that decides the course of action to take at any given instant.

Conservative Design Thinner oxides with smaller volumes and lower defect densities collect less charge. Thus, smaller geometries are more resilient to TID. However, other issues remain. At the MOSFET channel's edge, near the gate region boundary, two parasitic transistors are formed in parallel. In normal conditions, they are strongly cut-off and do not affect the device operation. But when irradiated, parasitic devices frequently have significant threshold voltage shifts. In both types, the threshold voltage decreases, which means that in the NMOS V_T becomes smaller and falls within the normal operating voltage of the device and in the PMOS V_T also becomes smaller, but increases in magnitude. Thus, the parasitic devices only contribute to excess leakage in the NMOS transistors. This issue can be bypassed by turning the transistor channel back around itself. The annular device structure, where the gate and the edge of the channel enclose the drain, eliminates the edge leakage path. The layout of a regular device and of an annular device is shown in figure 2.20, together with the respective responses to a certain dose of radiation.

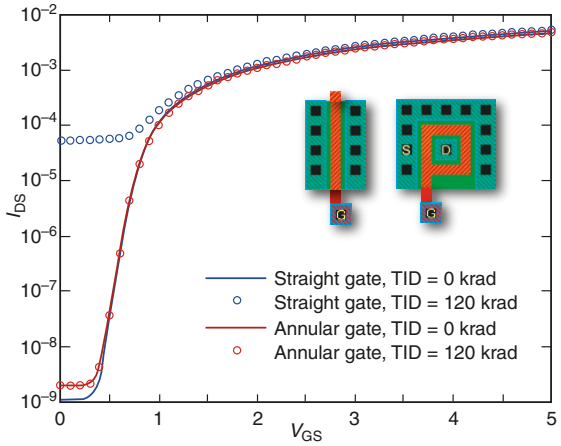

Figure 2.20: Drain current as a function of gate-source voltage for straight and annular *n*-channel MOSFETs [6].

The layout shown is one possible solution that provides radiation hardening features, which has some drawbacks, such as larger area, larger gate capacitance and greater drive strength. There are other layout solutions which are a variant of the one shown or approach the problem in a completely different way. These layout solutions can be used alone or be combined with other approaches to reinforce the radiation hardening features, such as the employment of guard rings to reduce or eliminate the latch-up sensitivity.

2.4.3 Capacitors

When a capacitor is subjected to radiation, the main cause of capacitance change is due to a variation in the inter-electrode spacing, induced by swelling of the structural materials. This change is more evident in capacitors built with organic materials. The changes in the dielectric constant of a capacitor's dielectric are limited or absent. The inside and surrounding air ionization, dielectric and filler material degradation and temperature increase, all due to incident radiation, may increase

the insulation resistance. Some types of capacitors, such as glass, mica and ceramic, display high insulation resistances and low dissipation factors. Other types, such as electrolytic and paper, exhibit low insulation resistances and high dissipation factors. So, the changes in the capacitance value and insulation resistance are considered first-order effects and changes in the capacitor's structure and dielectric constant are considered second-order effects, specially in capacitors made of inorganic dielectrics. A summary of radiation effects in different capacitor types is shown in figure 2.21.

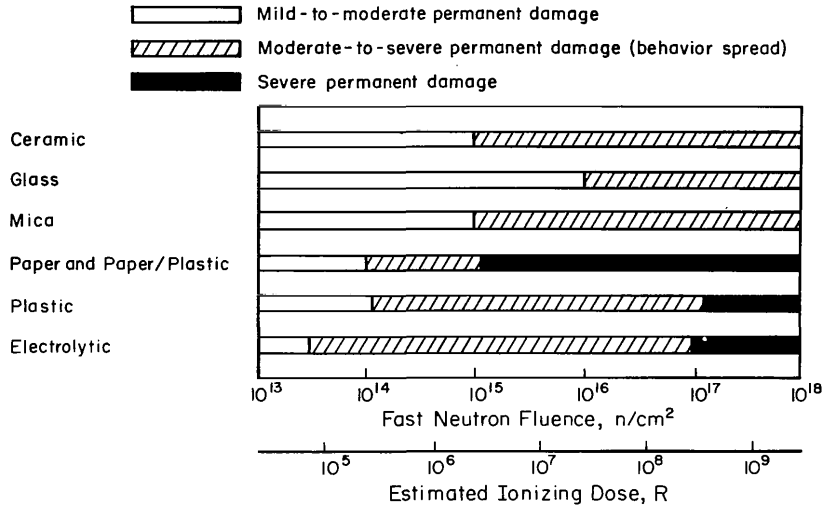

Figure 2.21: Relative radiation sensitivity of capacitors [7].

The permanent effects are a result of TID. The temporary changes that can occur due to irradiation induce capacitance changes that will be larger than the ones resulting from a permanent change. Thus, when a capacitor is employed in a nuclear or space environment, it is important to consider both temporary and permanent changes in the capacitor [7].

2.5 Radiation hardened converters

The effects of radiation depend on the converter topology, but parameters such as efficiency, converter output voltage, step response, loop gain frequency response or phase margin may be affected.

If the converter has a closed-loop regulation, the control part is also susceptible to radiation effects. In a fully analogue integrated PWM control composed by an amplifier, a comparator and a voltage reference, the most sensitive part is the internal voltage reference. A deviation in the voltage reference value may cause an unexpected operation. Also, some components, such as the comparator, may continue to operate after degradation due to radiation damage, but once the converter is powered down, they prevent a system restart and the converter ceases to function permanently [10].

If the control has a digital section, such as bistable elements or memory cells, their operation is likely to be affected by SEE, specially SEU, SET and SEFI. Eventually, they will also suffer from degradation due to TID.

For the off-chip capacitors, as it was seen in subsection 2.4.3, the dielectric material poses an important factor for the radiation hardness. The employment of glass capacitor is a good solution, since they have a reasonable radiation tolerance. But other capacitors with different dielectric materials, like mica or ceramic, can also be used.

Chapter 3

Theoretical Analysis

3.1 Series-parallel step-up DC-DC switched capacitor converter

A possible configuration for a series-parallel step-up DC-DC switched capacitor converter is shown in figure 3.1.

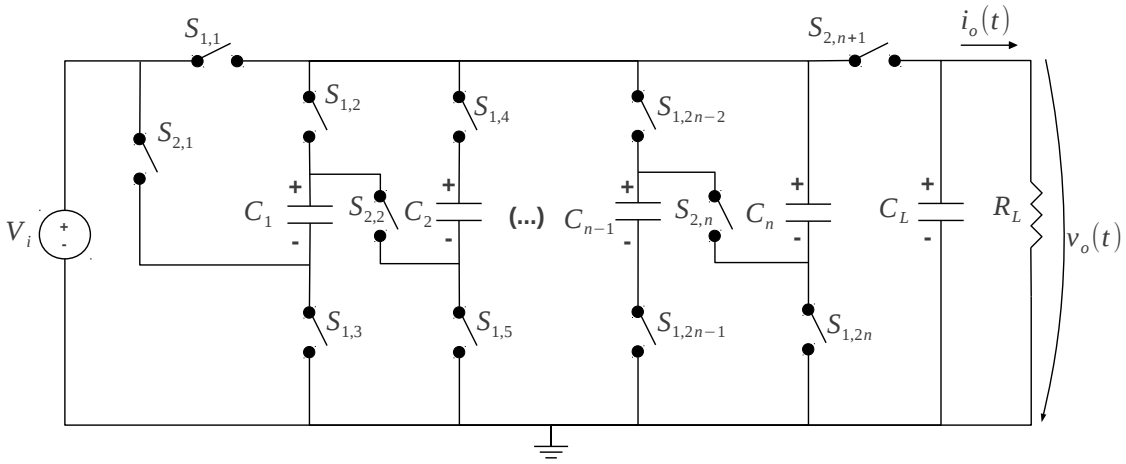

Figure 3.1: Series-parallel step-up DC-DC switched capacitor converter circuit.

In order to step the output voltage, the capacitors labelled $C_k|_{k\in[1,n]}$, also known as flying capacitors, are separated from the output and charged in parallel. Next, they are connected again with the output and discharged in series with the input. Before proceeding with the analysis of the converter, the following assumptions were made:

- n$\in \mathbb{N}$ represents the total number of flying capacitors in the circuit;
- The switches $S_{1,i}|_{i\in[1;2n]}$ and $S_{2,j}|_{j\in[1,n+1]}$ do not conduct simultaneously: when one set turns on, the other must turn or be already turned off;
- The switching frequency and the switching period are represented by f_s and T_s respectively;

- The duty-cycle is the switching period percentage that a given switch is on. The duty-cycle of the switches $S_{1,i}$ and $S_{2,j}$ is represented by D_{ϕ_1} and D_{ϕ_2} respectively, where D_{ϕ_1} and $D_{\phi_2} \in [0,1]$;

- Two different time concepts must be kept in mind. One, which will be called the operation time (t_o), is set to zero when the converter begins to operate and ends when mT_s s are reached, where $m \in \mathbb{N}$ is the number of operation cycles. Therefore, $t_o \in [0, mTs]$. And then, there is the relative time (t_{r1} and t_{r2}), which is set to zero whenever a switch turns on or off.

- The switches $S_{1,i}$ are on during $t_{r1} \in [0, D_{\phi_1} T_s[$, where $\Delta t_{r1} = D_{\phi_1} T_s$. The switches $S_{2,j}$ are on during $t_{r2} \in [0, D_{\phi_2} T_s[$, where $\Delta t_{r2} = D_{\phi_2} T_s$;

- Since the switches set $S_{1,i}$ and $S_{2,j}$ cannot be both on at the same time,

$$\Delta t_{r1} + \Delta t_{r2} \leq T_s \tag{3.1}$$

which also implies

$$D_{\phi_1} + D_{\phi_2} \leq 1 \tag{3.2}$$

3.1.1 Operation principles

During each switching cycle there are two operation stages. The first one occurs when the switches $S_{1,i}$ are on. The flying capacitors are rearranged as shown in figure 3.2 and are charged in parallel with the input. The second stage occurs when the switches $S_{2,j}$ are on. The flying capacitors become rearranged in series with each other, the input, the output and discharge the stored energy, as shown in figure 3.3. Their combined voltage, plus the input voltage allow the output voltage to be stepped.

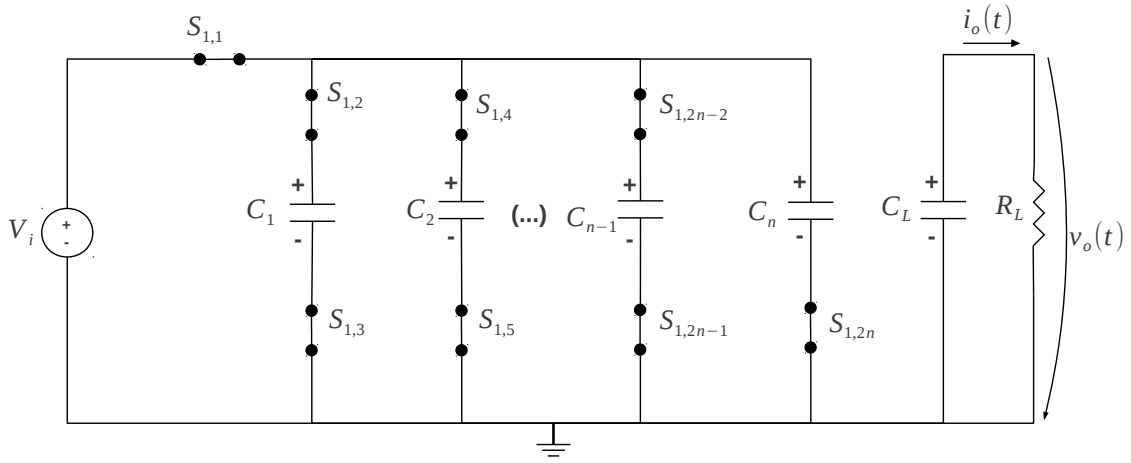

Figure 3.2: Equivalent circuit during stage 1 with ideal switches.

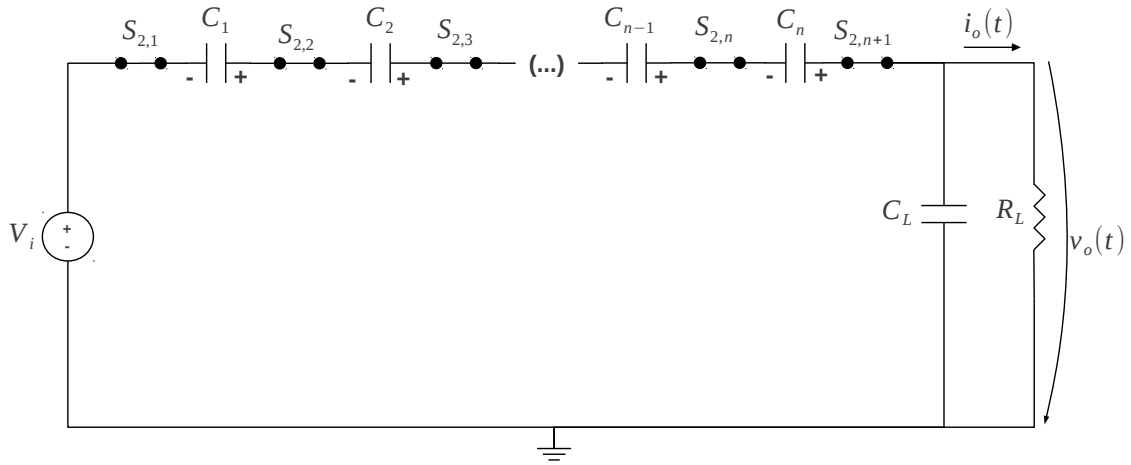

Figure 3.3: Equivalent circuit during stage 2 with ideal switches.

Ideally, the voltage conversion ratio is given by equation 3.3.

$$\frac{V_o}{V_i} = n+1 \tag{3.3}$$

However, the steady state value of the output voltage, as it will be seen in subsection 3.1.3, is restricted by the f_s-nC relationship, the on-resistance of the switches, the duty-cycle and the load capacitor (C_L) and resistance (R_L) values.

In CMOS technology, the switches are in fact MOSFETs. The deduction of the system model considering the actual MOSFETs can be very difficult, very time consuming and the unknown variables involved are so many that the model actually loses its usefulness. In the triode region, the MOSFET can be modelled as a voltage controlled resistor. So, that was the model chosen for the switches. In reality, the MOSFET resistance is not constant throughout the triode region operation, but in this analysis it will be assumed constant and corresponding to the maximum on-resistance of the semiconductor device. When the switches are off, hence the MOSFETs are not conducting, the resistance is considered infinite. Therefore, figures 3.2 and 3.3 are equivalent to 3.4 and 3.5 respectively.

3.1.2 Output and flying capacitors voltage

In figure 3.4 it is assumed that not all the switches have the same on-resistance. For the branches containing capacitors C_1 through C_{n-1}, each switch has an on-resistance equal to $\frac{r_{S1}}{2}$ and the remaining switches have an on-resistance of r_{S1}.

In the beginning of this study it was assumed that it was simpler to consider all the switches with the same on-resistance, but that approach led to the deduction of two different voltage expressions: $v_{C_{n-1}}(t)$ and $v_{C_n}(t)$, since different currents flow in the branches containing the capacitors. Besides, with this configuration, the number of poles in the circuit is two instead of one, which leads to longer and more complicated mathematical expressions. In addition, during stage two,

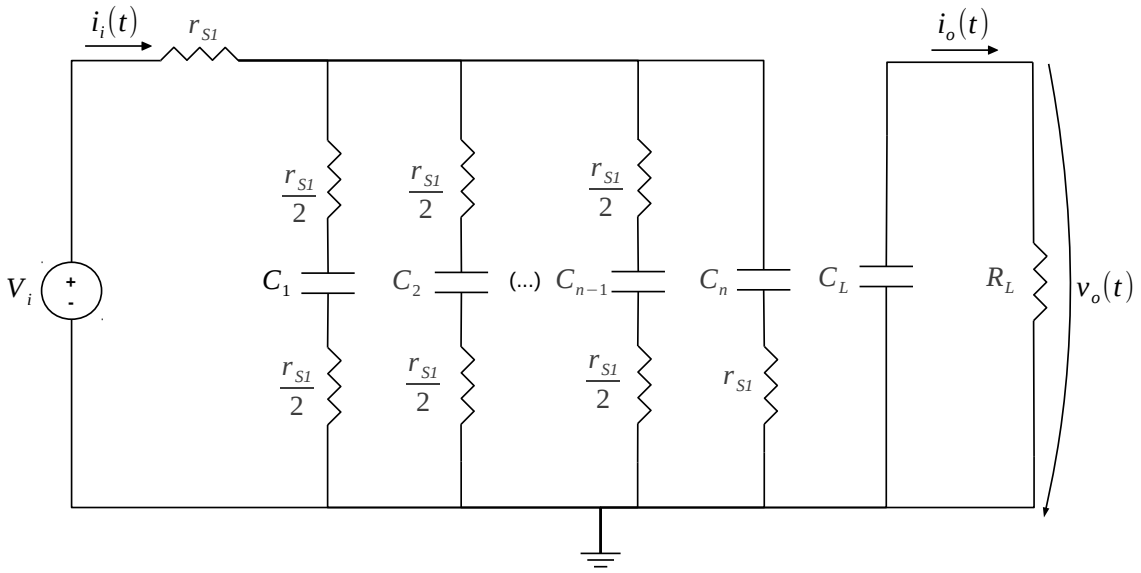

Figure 3.4: Equivalent circuit during stage 1 with non-ideal switches.

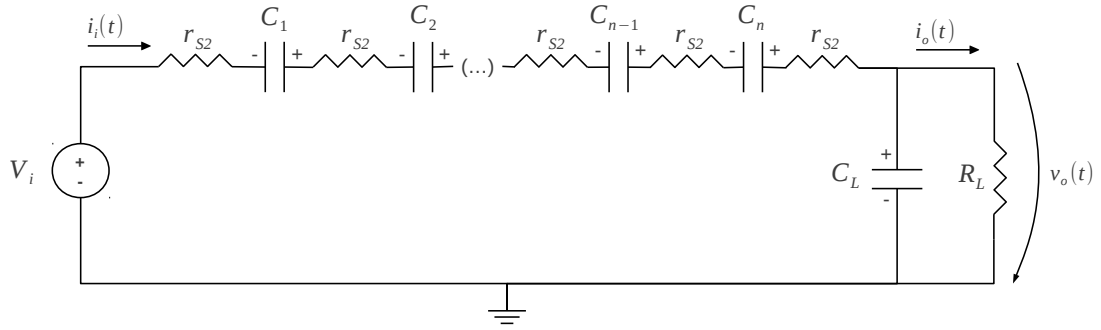

Figure 3.5: Equivalent circuit during stage 2 with non-ideal switches.

when the flying capacitors are in series, considering an ideal situation where there is no load, the steady state output voltage is given by $V_i + v_{C_{n-1}}(0^-)(n-1) + v_{C_n}(0^-)$ instead of $V_i + nv_{C_n}(0^-)$, which defeats the one of the main purposes of the circuit.

Since the switch resistance is a design parameter, with this approach, where two different on-resistances are considered, all capacitors are charged with the same current $i_C(t)$ and, therefore, all of them have the same voltage drop $v_C(t)$.

During a given switching period $k \in [0;m]$ where $m \in \mathbb{N}$, and considering that $D_{\phi_{1,k}}$ and $D_{\phi_{2,k}}$ are the duty-cycles of the switches involved in stage 1 and 2 respectively, the output and flying capacitors voltages are given by

Stage 1: $[(k-1)T_s;(k-1)T_s+D_kT_s[$

$$v_{o1_k}(t_{r1}) = v_{o1_k}(0^-)e^{-t_{r1}p_2} \tag{3.4}$$
$$v_{C1_k}(t_{r1}) = v_{C1_k}(0^-)e^{-t_{r1}p_1} + V_i(1-e^{-t_{r1}p_1}) \tag{3.5}$$

for $0 \leq t_{r1} < D_{\phi_{1,k}}T_s$.

During stage 2: $[(k-1)T_s+(1-D_{\phi_{2,k}})T_s;kT_s[$

$$v_{o2_k}(t_{r2}) = K_1\left[(e^{t_{r2}p_3}-e^{t_{r2}p_4})(V_i+nv_{C2_k}(0^-)) + (H_1e^{t_{r2}p_3}-H_2e^{t_{r2}p_4})v_{o2_k}(0^-)\right] \tag{3.6}$$
$$\begin{aligned} v_{C2_k}(t_{r2}) =& K_2[M_1nv_{C_k}(0^-) - (M_2+M_3e^{t_{r2}p_3}-M_4e^{t_{r2}p_4})(V_i+nv_{C2_k}(0^-)) \\ & - (M_5+M_6e^{t_{r2}p_3}-M_7e^{t_{r2}p_4})v_{o2_k}(0^-)] \end{aligned} \tag{3.7}$$

for $0 \leq t_{r2} < D_{\phi_{2,k}}T_s$, where

$$G_1 = \frac{nC_L}{C} \qquad K_1 = \frac{\frac{1}{G_1G_3}}{p_3-p_4}$$
$$G_2 = \frac{1}{R_LC_L} \qquad K_2 = \frac{\frac{1}{G_1}}{n(p_3-p_4)}$$
$$G_3 = \frac{(n+1)}{n}r_{S2}C$$

$$H_1 = G_1(G_3p_3+1)$$
$$H_2 = G_1(G_3p_4+1)$$

$$M_1 = G_3(p_3-p_4) \qquad M_5 = \frac{p_3-p_4}{p_3p_4}$$
$$M_2 = \frac{p_3-p_4}{p_3p_4}G_2 \qquad M_6 = \frac{1}{p_3}G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)$$
$$M_3 = \frac{G_2+p_3}{p_3} \qquad M_7 = \frac{1}{p_4}G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)$$
$$M_4 = \frac{G_2+p_4}{p_4}$$

$$p_1 = \frac{1}{(n+1)r_{S1}C} \qquad p_2 = \frac{1}{R_LC_L}$$

$$p_{3,4} = \frac{1}{2}\left(-\frac{G_1G_2G_3+G_1+1}{G_1G_3} \pm \sqrt{\left(\frac{G_1G_2G_3+G_1+1}{G_1G_3}\right)^2 - 4\frac{G_2}{G_3}}\right)$$

For a detailed description about the deduction of equations 3.4 to 3.7 see appendix B. For m cycles, the output and flying capacitors voltage is given by

$$v_o(t_o) = \begin{cases} v_{o1_1}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{1,1}}T_s & \text{and} & 0 \le t_o < D_{\phi_{1,1}}T_s \\ v_{o2_1}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,1}}T_s & \text{and} & (1-D_{\phi_{2,1}})T_s \le t_o < T_s \\ \quad\vdots & & & \\ v_{o1_k}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{1,k}}T_s & \text{and} & (k-1)T_s \le t_o < (k-1)T_s + D_{\phi_{1,k}}T_s \\ v_{o2_k}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,k}}T_s & \text{and} & (k-1)T_s + (1-D_{\phi_{2,k}})T_s \le t_o < kT_s \\ \quad\vdots & & & \\ v_{o1_m}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{2,m}}T_s & \text{and} & (m-1)T_s \le t_o < (m-1)T_s + D_{\phi_{1,m}}T_s \\ v_{o2_m}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,m}}T_s & \text{and} & (m-1)T_s + (1-D_{\phi_{2,m}})T_s \le t_o < mT_s \end{cases} \tag{3.8}$$

$$v_C(t_o) = \begin{cases} v_{C1_1}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{1,1}}T_s & \text{and} & 0 \le t_o < D_{\phi_{1,1}}T_s \\ v_{C2_1}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,1}}T_s & \text{and} & (1-D_{\phi_{2,1}})T_s \le t_o < T_s \\ \quad\vdots & & & \\ v_{C1_k}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{1,k}}T_s & \text{and} & (k-1)T_s \le t_o < (k-1)T_s + D_{\phi_{1,k}}T_s \\ v_{C2_k}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,k}}T_s & \text{and} & (k-1)T_s + (1-D_{\phi_{2,k}})T_s \le t_o < kT_s \\ \quad\vdots & & & \\ v_{C1_m}(t_{r1}) & \text{for} \quad 0 \le t_{r1} < D_{\phi_{2,m}}T_s & \text{and} & (m-1)T_s \le t_o < (m-1)T_s + D_{\phi_{1,m}}T_s \\ v_{C2_m}(t_{r2}) & \text{for} \quad 0 \le t_{r2} < D_{\phi_{2,m}}T_s & \text{and} & (m-1)T_s + (1-D_{\phi_{2,m}})T_s \le t_o < mT_s \end{cases} \tag{3.9}$$

3.1.2.1 Maximum and minimum flying capacitors voltage values

Analysing circuit from figure 3.4, the following equation can be drawn:

$$v_C(t) = V_i - nr_{S1}\frac{d}{dt}v_C(t) - r_{S1}\frac{d}{dt}v_C(t) = V_i - (n+1)r_{S1}\frac{d}{dt}v_C(t) \tag{3.10}$$

When the capacitors are fully charged, no current flows trough the switches, since $v_C(t) = V_{C_{max}} = constant$ and therefore $\frac{d}{dt}v_C(t) = 0$. Hence,

$$V_{C_{max}} = V_i \tag{3.11}$$

Analysing the circuit from figure 3.5, the following equation can be drawn:

$$V_i + (n+1) r_{S2} \frac{d}{dt} v_C(t) + n v_C(t) = v_o(t) \tag{3.12}$$

When the capacitors are fully discharged, no current flows trough the resistors, since $v_C(t) = V_{C_{min}}$ and therefore $\frac{d}{dt} v_C(t) = 0$. Assuming that when the flying capacitors discharge, the output has a constant value of $v_o(t) = V_o$, the flying capacitors minimum voltage is given by equation 3.13.

$$V_{C_{min}} = \frac{V_o - V_i}{n} \tag{3.13}$$

So, even if the flying capacitors fully discharge, their voltage drop $v_C(t)$ is only zero when $V_i = V_o$. During the steady state they have always a positive value.

3.1.2.2 Flying capacitors charging and discharging considerations

If a flying capacitor has time to fully charge and discharge, there are essentially two possible voltage waveforms, which are represented in figures 3.6 and 3.7.

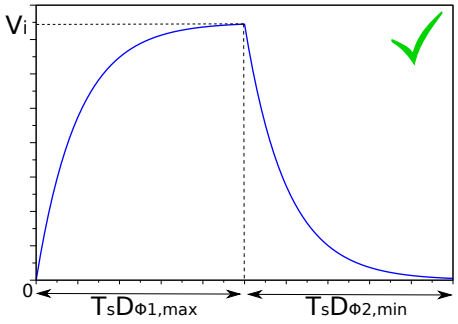

Figure 3.6: Flying capacitors advisable and most desirable charging and discharging waveform.

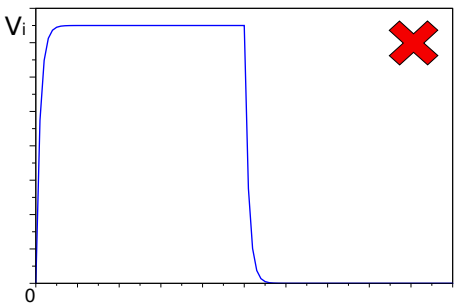

Figure 3.7: Flying capacitors inadvisable and avoided charging and discharging waveform.

$D_{\phi_{1,max}}$ and $D_{\phi_{2,min}}$ correspond to the maximum and minimum duty-cycle values of ϕ_1 and ϕ_2 respectively, which allow the flying capacitors to charge from 0 to V_i and fully discharge.

If the capacitors are charged in the way shown in 3.7, since the voltage variation occurs very fast, large currents may be generated during the charging process, which can be very harmful to the circuit. By charging and discharging the capacitors as shown figure in 3.6, there is a smoother transition between voltage levels, and the rush currents will have a much smaller magnitude.

Also, this method allows a more precise control of the energy transfer between the input and output, since $v_C(t)$ and $v_o(t)$ become dependent of D_{ϕ_1} and/or D_{ϕ_2}.

For instance, by manipulating D_{ϕ_1}, it is possible to directly control the flying capacitors charge-up voltage, as shown in figure 3.8. From this figure, it is clear that a lower D_{ϕ_1} corresponds to

$v_C(D_{\phi_1}T_s) = V_a < V_i$, showing that increasing or lowering D_{ϕ_1} influences the charge-up value of $v_C(t)$ and allows the output voltage regulation.

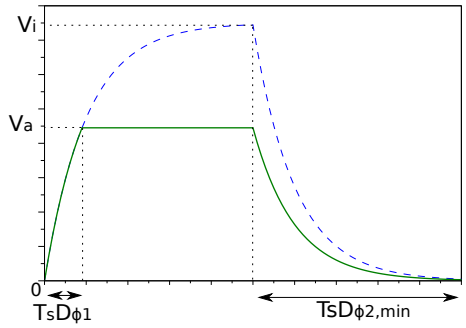

Figure 3.8: Flying capacitors voltage waveform for $D_{\phi_1} < D_{\phi_1,max}$.

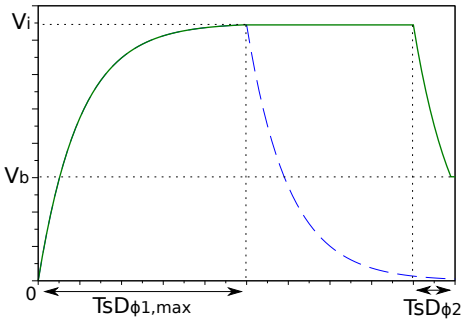

Figure 3.9: Flying capacitors voltage waveform for $D_{\phi_2} < D_{\phi_2,min}$.

By increasing D_{ϕ_2}, the capacitors are no longer able to fully discharge. The amount of charge transferred from the input to the output can be controlled, since at the end of T_s, the flying capacitors will have a different voltage drop, $v_C(T_s) = V_b > 0$, as shown in figure 3.9. This way, the output voltage can be controlled by manipulating either D_{ϕ_1}, D_{ϕ_2} or by an eventual combination of the two, but always keeping in mind the restrictions imposed by equations 3.1 and 3.2. All depends on the designer's option and the chosen control method.

3.1.3 Voltage conversion ratio

Considering $R_L \to \infty$, then

$$G_2 = \frac{1}{R_L C_L} \to 0 \tag{3.14}$$

$$p_3 = \frac{1}{2}\left(-\frac{G_1G_2G_3 + G_1 + 1}{G_1G_3} + \sqrt{\left(\frac{G_1G_2G_3 + G_1 + 1}{G_1G_3}\right)^2 - 4\frac{G_2}{G_3}}\right) \to 0 \tag{3.15}$$

$$p_4 = \frac{1}{2}\left(-\frac{G_1G_2G_3 + G_1 + 1}{G_1G_3} + \sqrt{\left(\frac{G_1G_2G_3 + G_1 + 1}{G_1G_3}\right)^2 - 4\frac{G_2}{G_3}}\right) \to -\frac{G_1 + 1}{G_1G_3} \tag{3.16}$$

$$H_1 = G_1(G_3p_3 + 1) \to G_1 \tag{3.17}$$

$$K_1 = \frac{\frac{1}{G_1 G_3}}{p_3 - p_4} \rightarrow G_1 + 1 = \frac{nC_L}{C} + 1 = \frac{nC_L + C}{C} \tag{3.18}$$

With these assumptions, the output voltage during stage 2 can be approximated by equation 3.19.

$$v_o(t) \backsimeq \frac{nC_L + C}{C} \left[(1 - e^{tp_4})(V_i + nv_C(0^-)) + (G_1 - H_2 e^{tp_4}) v_o(0^-) \right] \tag{3.19}$$

The previous expression contains exponential elements. The only way to eliminate them is neglecting the load capacitor. Considering that $C_L \rightarrow 0$

$$G_1 = \frac{nC_L}{C} \rightarrow 0 \tag{3.20}$$

$$p_4 \rightarrow -\frac{G_1 + 1}{G_1 G_3} \rightarrow \infty \tag{3.21}$$

$$K_1 \rightarrow \frac{nC_L}{C} + 1 \rightarrow 1 \tag{3.22}$$

Thus, the output voltage can be approximated by equation 3.23.

$$v_o(t) \backsimeq V_i + nv_C(0^-) \tag{3.23}$$

Considering that during stage 1 the flying capacitors are allowed to charge to their maximum voltage which is $v_C(0^-) = V_i$, the output voltage ceases to be a function of time and becomes a constant which is only dependent of the DC input voltage magnitude and the number of flying capacitors.

$$V_o = (n+1)V_i \tag{3.24}$$

Which means that the voltage conversion ratio is given by

$$\frac{V_o}{V_i} = n + 1 \tag{3.25}$$

As it can be seen from the previous deduction, this voltage ratio is ideal. A number of assumptions and simplifications were made. Summarizing, the voltage ratio described in equation 3.25 is only valid when:

- $v_C(0^-) = V_i$;
- $R_L \rightarrow \infty$;

- $C_L \to 0$.

In reality, since by design the C_L capacitor cannot be eliminated when no load is present and usually, despite the fact that the converter can and may operate with no load, the converter is generally designed for a specific purpose, for a certain operating point where a certain load value is expected. So, equation 3.25 represents the maximum conversion ratio of the converter. The real conversion ratio is limited by the load capacitor and resistor values, switch on-resistance, flying capacitors value and number, the duty-cycle and by the f_s-nC relationship, as it will be shown in the next subsection.

3.1.3.1 Ideal vs real voltage conversion ratio

The following plots were made with the open source software Scilab. The used functions and the main program source code can be found in appendix C. The values used to perform each plot (f_s, D_{ϕ_1}, D_{ϕ_2}, m, V_i, n, C, r_{S1}, r_{S2}, C_L and R_L) were chosen in order to exemplify clearly every situation. The developed computational program only contemplates an open-loop control. Therefore, in each example, the duty-cycle of the switches is assumed constant.

In the previous section, based on the mathematical model of the converter, a series of simplifications and assumptions were made in order to obtain the ideal voltage conversion ratio of a typical series-parallel switched capacitor step-up DC-DC converter. It was stated that the voltage conversion ratio was $\frac{V_o}{V_i} = n+1$ when no load (both R_L and C_L) are present in the circuit and the flying capacitors are allowed to charge from 0 to V_i in $D_{\phi_1} T_s$ s. In the present subsection the reverse process is applied. The analysis will begin with no load. Gradually, the components will be added and the effects on the output response properly analysed. Unless stated otherwise, the used values are indicated in table 3.1.

Table 3.1: Main values used to perform the output and flying capacitors voltage plots.

f_s	10 MHz
V_i	1 V
D_{ϕ_1}	50 %
D_{ϕ_2}	50 %
n	2
C	20 nF
r_{S1}	0.15 Ω
r_{S2}	0.25 Ω
R_L	50 kΩ
C_L	1 fF

In figure 3.10 both the output and flying capacitors voltage when $R_L \simeq \infty$ and $C_L \simeq 0$ are represented. A converter operating in these conditions would show a mean output voltage given by

$$V_o = (n+1)V_i = (2+1) \times 1 = 3\text{V}$$

The values listed for C_L and R_L are not actually 0 or ∞, since these values turn the computations unfeasible, but if they are large or small enough relatively to the other component values, they can be assumed to be very close to 0 or ∞.

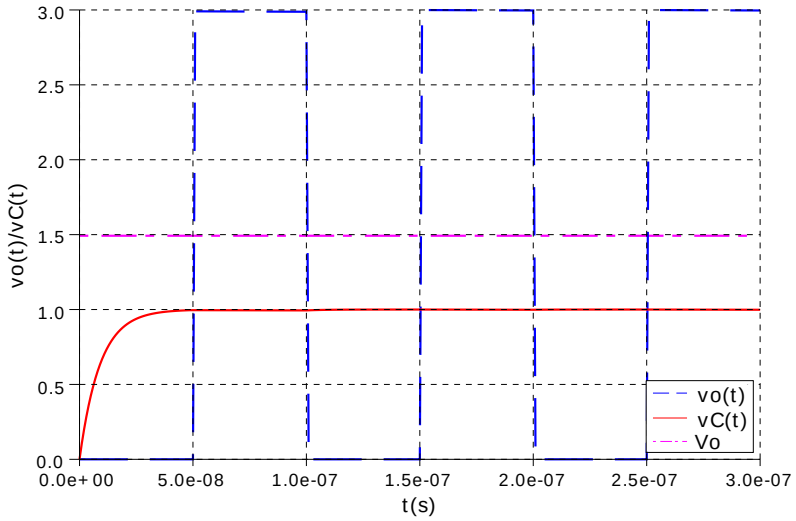

Figure 3.10: $v_o(t)$ and $v_C(t)$ waveforms with no C_L and R_L present at the output.

From figure 3.10, it can be seen that the output voltage does not remain constant during the operation of the converter. In fact, when the output is disconnected from the source, the output voltage drops to 0 V. Thus, the actual mean value is 1.5 V and not 3 V. To achieve the mean value of 3 V during steady state, the duty-cycle would have to be large in the first cycle, since the flying capacitors need time to charge at least once, and 0 in the remaining ones. But, in reality, a converter which only assures the desired output voltage if no load current is supplied is not very useful. Maintaining all the other parameters and introducing a finite load resistor of 50 Ω in the circuit generates a response depicted in figure 3.11.

The issues shown in figure 3.10 remain. When the output is disconnected from the source the output voltage drops to 0 V which drives the actual output mean value well below 3 V. Besides, the addition of a load resistance lowered the peak output voltage and the ideal voltage is now never reached, making the mean value lower than 1.5 V.

To maintain a constant output value during the steady state, even when the output is disconnected from the source, a load capacitor is usually employed. To begin the analysis of the C_L influence, the load resistor was considered again absent and $C_L = 100$ nF. The results are depicted in figure 3.12.

From this figure, it can be seen that the output voltage reaches 3 V, but it takes some time because the load capacitor has to be charged. From the $v_o(t)$ transient time it can be seen that capacitor C_L is charged with a time constant of $\simeq 1$ μs, corresponding to charging through a resistance of 10 Ω. This result is coherent with the well known behaviour of the switched capacitor circuits based on the fact that a capacitor C switched at a frequency f=1/T, is equivalent to a resistor

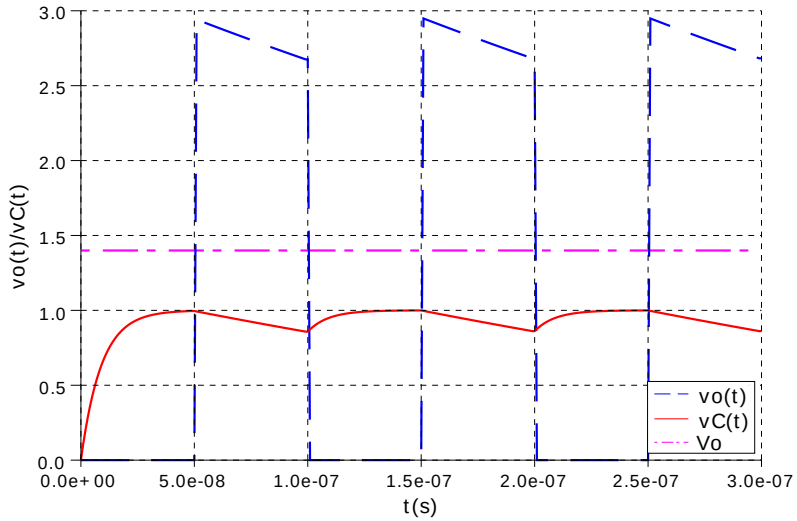

Figure 3.11: $v_o(t)$ and $v_C(t)$ waveforms with $R_L = 50\ \Omega$ and no C_L present at the output.

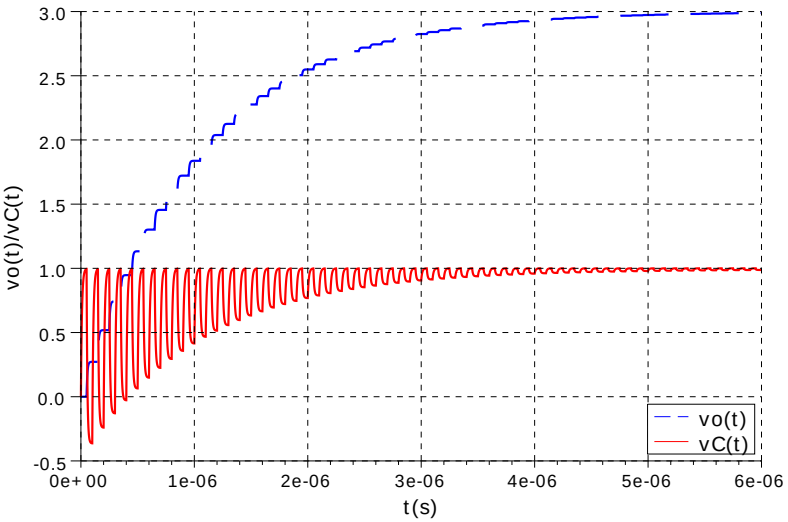

Figure 3.12: $v_o(t)$ and $v_C(t)$ waveforms with $C_L = 100$ nF and no R_L present at the output.

of value T/C. It is of notice that in the discharging period, the two capacitors are in series, and thus, present a value of 10 nF. Maintaining all the other parameters and introducing again load resistor of 50 Ω in the circuit generates the response shown in figure 3.13.

The load resistor has a significant influence in the voltage conversion ratio. From figure 3.11 it is clear that the load resistor lowers the output voltage. Even if the output voltage did not drop to o V when the load is disconnected from the source and assuming that during that time it somehow remained constant, the mean value should be around 2.7 V. However, when the load resistor is put in parallel with a capacitor, the mean voltage dropped to 2.5 V. The load capacitor is not a critical

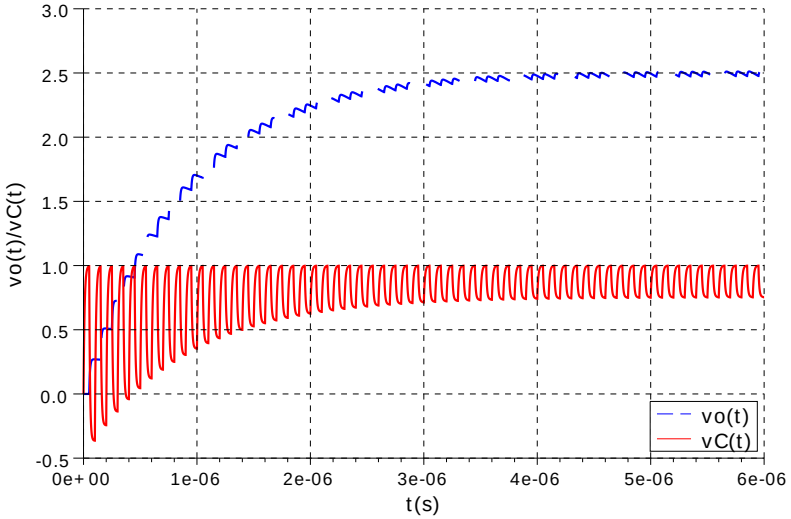

Figure 3.13: $v_o(t)$ and $v_C(t)$ waveforms for $R_L = 50\ \Omega$ and $C_L = 100$ nF.

functional element. It was shown that the converter is fully capable of stepping the input voltage without it. When employed in the load alone it has no significant effect in the mean output value. Some authors omit C_L from their equations to simplify the analysis, but, besides establishing the output voltage ripple and influencing the response time, also influences the steady state mean value of the output voltage when employed in parallel with a resistive load. Thus, its inclusion in the model of the converter is important

With the inclusion of a load capacitor, another factor has to be taken into account. Since the capacitor has to be supplied with a certain amount of charge every period, the input needs to have the capability of providing enough energy to achieve and maintain the desired output voltage mean value. For a given C_L, the relation between the flying capacitors number and size and the switching frequency, influences the converter energy transfer capabilities. For instance, by reducing the capacitance of C to 10 nF, the converter response is given by figure 3.14.

By lowering C, the input ceases to have the ability to transfer the necessary amount of energy required by the output to successfully step the voltage. If the load resistor was absent, it could take some time, but the load capacitor would eventually charge, since there were no dissipative elements attached to it. This can be seen in figure 3.15 where no R_L was considered and was used C = 1 nF.

So, why, if employed separately, the converter reaches 3 V during steady state, and it does not when R_L and C_L are employed in parallel? When stage 1 takes place, C_L is no longer able to preserve its own charge since some energy is discharged trough R_L. Since the load capacitor experiences charge losses during this stage, when stage 2 occurs, the flying capacitors need to have the ability to restore the amount of charge lost during stage 1 and simultaneously provide some energy to R_L in order to keep a constant load current flowing. If the C_L rate of charge is smaller than the rate of discharge, the output may never reach the desired value.

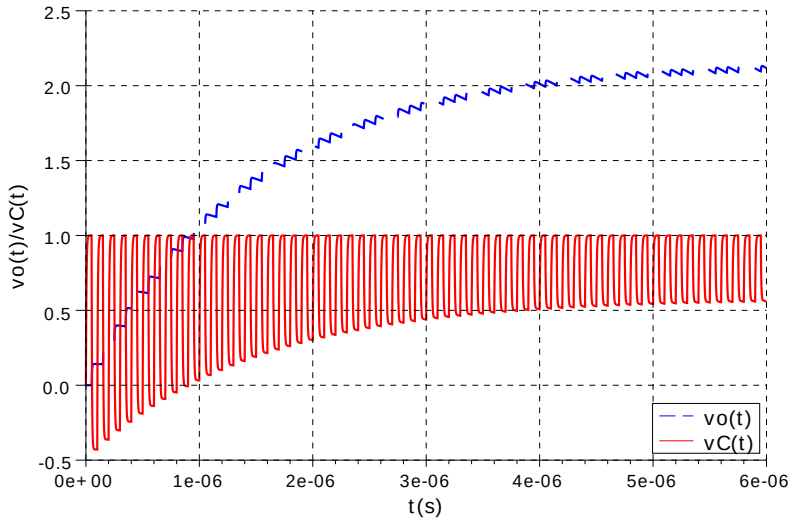

Figure 3.14: $v_o(t)$ and $v_C(t)$ waveforms for $R_L = 50\ \Omega$, $C_L = 100$ nF and C = 10 nF.

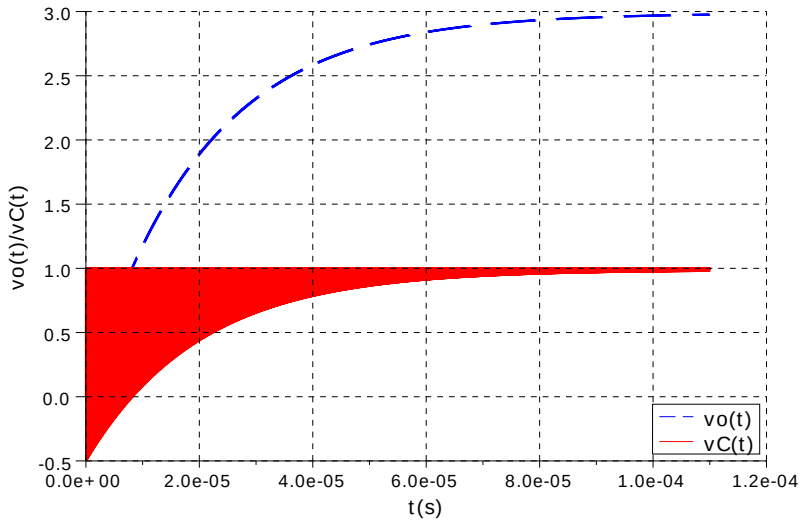

Figure 3.15: $v_o(t)$ and $v_C(t)$ waveforms for $C_L = 100$ nF, C = 1 nF and no R_L present at the output.

One way of increasing the energy provided by the input is raising the value of the flying capacitors to C = 1000 nF = 1 μF. But to allow the flying capacitors to fully charge and discharge it is necessary to lower the switches on-resistance to $r_{S1} = 0.002\ \Omega$ and $r_{S1} = 0.04\ \Omega$. The results are shown in figure 3.16.

From this figure it is clear that the mean output voltage value is very near 3 V during the steady state. But to achieve such results, C has to be 50 times larger and the value of the switches on-resistance has to be much smaller. Until now, the theoretical analysis has mainly addressed the voltage drops in the circuit, but the study of the current flow, specially the current magnitudes,

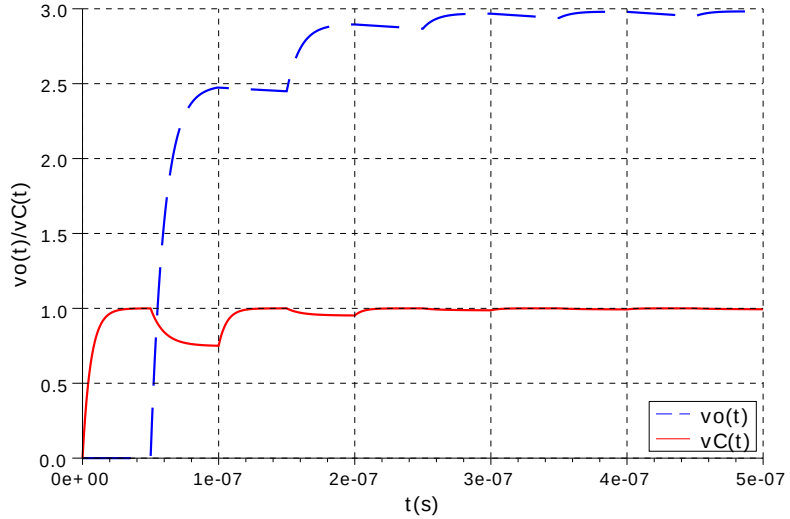

Figure 3.16: $v_o(t)$ and $v_C(t)$ waveforms for $R_L = 50\ \Omega$, $C_L = 100$ nF and C = 1 μF.

is an important subject. And the size of some system components have a great influence in the current value. This subject will be approached later, but is important to keep in mind that there are several advantages if the value of the on-resistance is maximized. Another way to achieve the 3 V maintaining C = 20 nF is by increasing the switching frequency. This way the flying capacitors discharge energy more often and the load itself has less time to discharge when disconnected from the source. However, since an increase in frequency also implies a decrease in the switching period, the flying capacitors will have less time to charge and, therefore achieves the same voltage in less time. The value of the switches on-resistance would also have to be lowered.

A different (illustrative) solution is increasing the flying capacitors number to n=3 maintaining C = 20 nF, $C_L = 100$ nF, $R_L = 50\ \Omega$ and $r_{S2} = 0.25\ \Omega$. It only requires adjusting the switch on-resistance $r_{S1} = 0.25\ \Omega$ to prevent the flying capacitors to fully charge, because now if they did so, the output voltage would actually exceed 3 V. With these new values, the converter response is the one depicted in figure 3.17.

In conclusion, in the previous section it was seen that several assumptions and simplifications have to be made in order to obtain the voltage conversion ratio $\frac{V_i}{V_o} = n + 1$. In this subsection it was verified, through the analysis of a series of voltage plots which covered several situations, that those simplifications are not realistic, which makes such voltage conversion ratio ideal. It was shown that the real voltage conversion ratio is not only dependent of n, but is also dependent of f_s, C, r_{S1}, r_{S2}, C_L and R_L. None of these elements can be assumed absent, because it is the interaction between them that actually defines the value of the output voltage. If one of them is deliberately ignored from the model, the results obtained are less accurate. The model described in the beginning of the section is by itself an approximation of reality. The real model of the converter is extremely complex and has hundreds of variables. So, further approximations, such as suppressing C_L or R_L, unnecessarily increase the gap between the two models. Thus, the ideal

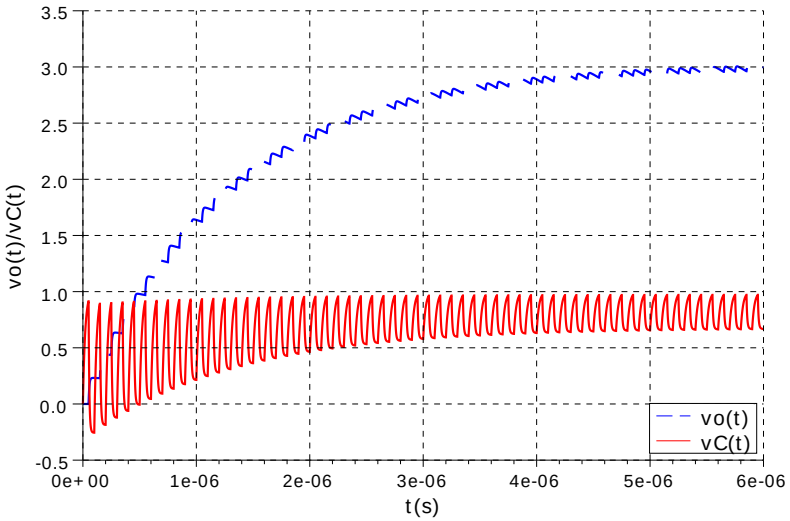

Figure 3.17: $v_o(t)$ and $v_C(t)$ waveforms for $R_L = 50\ \Omega$, $C_L = 100$ nF and n = 3.

voltage conversion ratio can be used in the beginning of the converter design as a reference, but once the circuit parameters are established, the real and ideal voltage conversion ratios cannot be expected to match.

3.1.3.2 Duty-cycle influence in the output voltage

In the previous subsection the effects of n, f_s, C, r_{S1}, r_{S2}, C_L and R_L in the output voltage were studied, always considering that the flying capacitors were able to fully charge and discharge. In this subsection the effects of D_{ϕ_1} and D_{ϕ_2} in the steady state output mean voltage are analysed, considering all the other circuit variables constant.

Consider the illustrative example depicted in figure 3.18, where D_{ϕ_2} = 100 - D_{ϕ_1}. In this example, beyond $D_{\phi_1} = 60\%$ the steady state output voltage begins to decrease. The flying capacitors have the same or a higher level of charge, since D_{ϕ_1} increases, but they cease to have time to discharge, and therefore the output voltage value drops. One way of preventing this situation is making D_{ϕ_2} constant and limiting the value of D_{ϕ_1} to $D_{\phi_{1,max}} = 100 - D_{\phi_2}$.

3.1.4 Converter design

As it was stated before, the main goal of the converter is to step the input voltage, which has a predefined range of $V_i \in [0.9; 1.5]$ V, to an output voltage of 2.5 V. Therefore, the maximum voltage conversion ratio is given by

$$M_{max} = \frac{V_o}{V_{i_{min}}} = \frac{2.5}{0.9} \simeq 2.8 \tag{3.26}$$

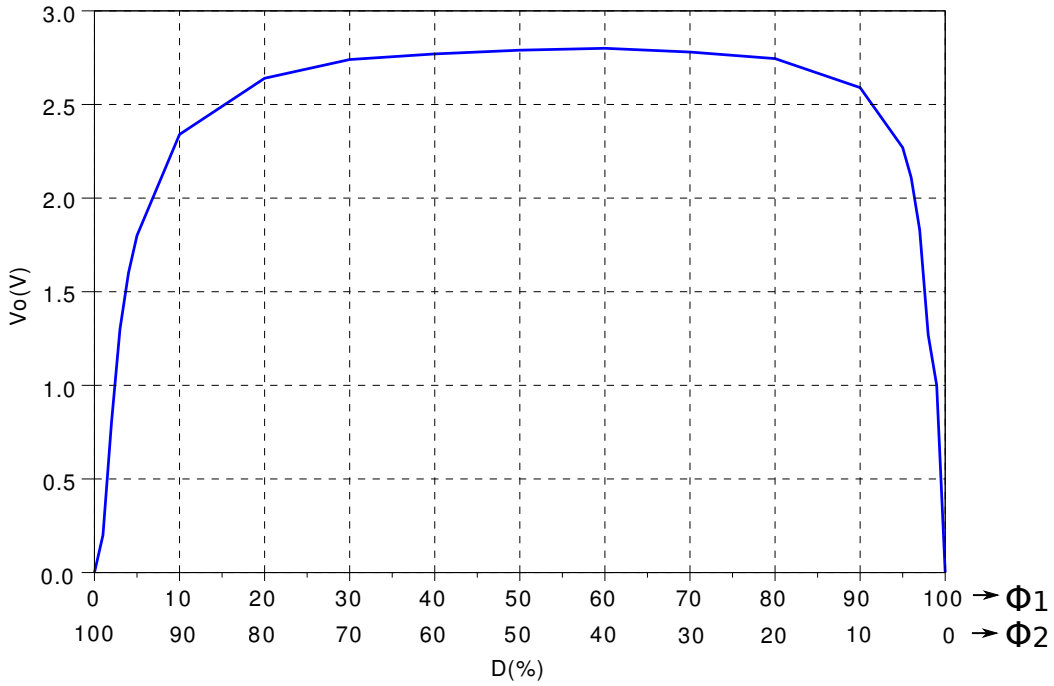

Figure 3.18: Steady state output voltage versus the duty-cycle.

Considering, as a starting point, the ideal voltage conversion ratio given by equation 3.25, the minimum number of flying capacitors that ensures a voltage step higher than M_{max} is $n = 2$, since

$$M = n + 1 = 2 + 1 = 3$$

With only two capacitors, for $V_i = 0.9$ V the maximum output voltage is $V_o = 3 \times 0.9 = 2.7$ V which is very close to the desired output value. Considering that in real systems energy losses occur due to non-ideal behaviour, the converter was designed with three flying capacitors instead of two, ensuring a maximum output voltage of $V_o = 4 \times 0.9 = 3.6$ V for $V_i = 0.9$ V, which allows more manoeuvrability in the converter design and control.

The empirical determination of the converter parameters can be difficult and very time consuming. Hand calculations can be extensive and if some parameters change, which is very common during the design process, such calculations have to be remade several times, which can also be time consuming. So, a parameter extraction program based on the mathematical model deduced was developed. The source code can be found in appendix C, section C.2. A flowchart is depicted in figure 3.19.

Since the design was based on a iterative process, which can be computationally demanding if the number of variables is too large, some of the parameters where previously established, such as the switching frequency, maximum and minimum switch duty-cycles. The flying capacitors voltage, switch on-resistance and load capacitors were computed.

As it was seen in subsection 3.1.3.1, if not excessively large, the load capacitor does not change

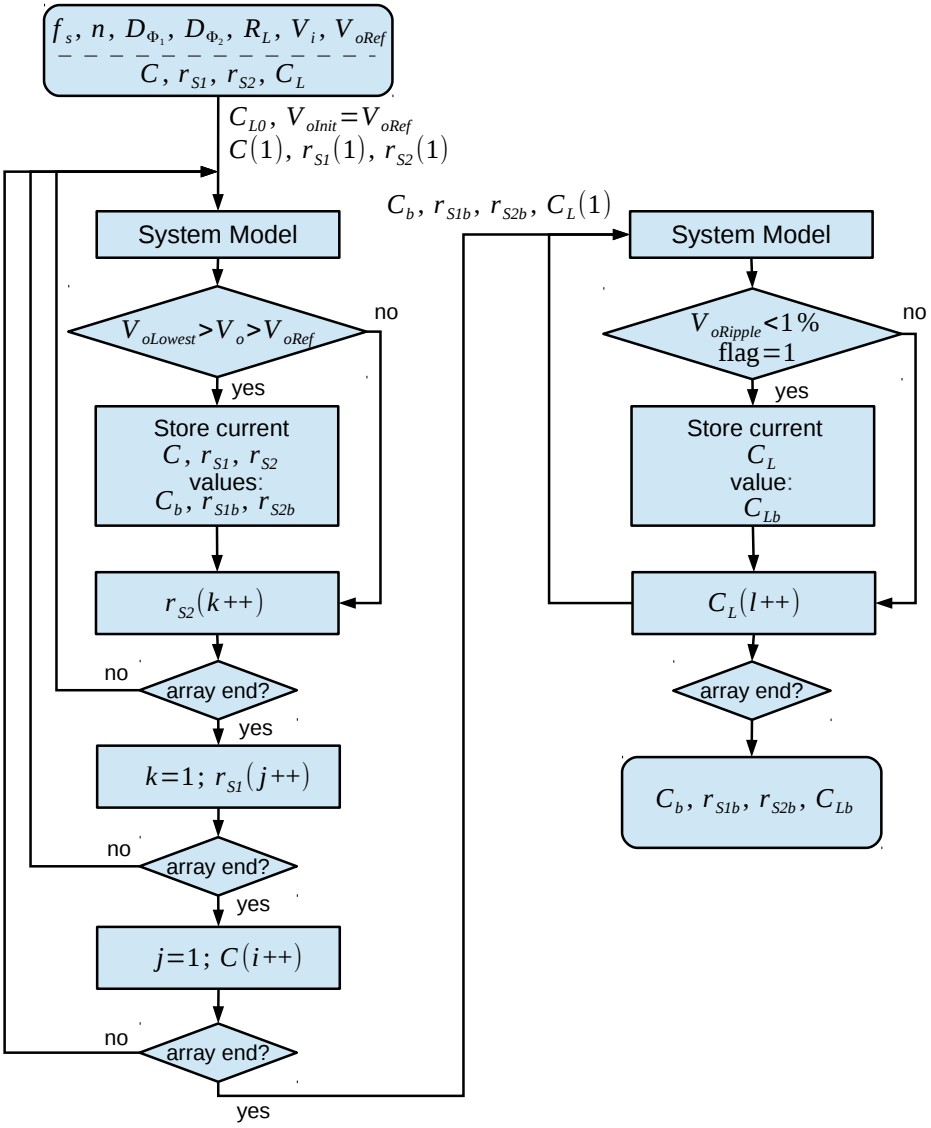

Figure 3.19: Converter design flowchart.

the steady state output voltage. It has a more significant influence in the voltage settling time and ripple. Therefore, in the beginning of the design, the load capacitor was set with a temporary value of $C_{L0} = 500$ nF. To make the design process faster, the operation in steady state was analysed and therefore, $V_{oInit} = V_{oRef}$. C, r_{S1}, r_{S2} and C_L are arrays with a given range. In the beginning of the program, the points are at the start of the arrays and then are incremented when needed. The model is run for all possible combinations of C, r_{S1}, r_{S2} and the DC output voltage value is analysed. Every time the resulting DC output voltage is above V_{oRef} and is simultaneously smaller than the previous best (smaller) result, the current values of C, r_{S1}, r_{S2} are stored. When all the elements of the arrays are used in the model, the C_L value is calculated. The process is repeated, but this time C, r_{S1}, r_{S2} are assumed constant, with the values obtained in the first part of the computation

process and the C_L array is swept. The first time that 1 % ripple is achieved, the corresponding C_L value is stored. The following values are not stored because a smaller capacitor is preferred.

The system was designed for $V_i = 0.9$ V, which was somewhat inconvenient but necessary, since considerably larger capacitor and a smaller on-resistance values were attained, compared to the ones obtained if the system was dimensioned considering the nominal input voltage. Besides, in open-loop if the converter can reach an output voltage of 2.5 V with an input voltage of 0.9 V, it will reach higher values for larger input voltages. Therefore, in order to assure a good line regulation, the converter has to be designed for $V_i = 0.9$ V. The input values used and the design results are shown in figure 3.20.

```
fs = 10e6;                    // Switching frequency (Hz)
D1 = 70;                      // Duty-cycle of phi1 (%)
D2 = 30;                      // Duty-cycle of phi2 (%)
m1 = 50;                      // Number of operation cycles

Vi = 0.9;                     // Input voltage (V)
n = 3;                        // Number of flying capacitors

VoRef = 2.5;                  // Reference output voltage (V)
IoRef =100e-3;                // Reference output current (A)
VoRipple = 0.01*2.5;          // Desired voltage ripple

C  = 65e-9:1e-9:70e-9;        // Flying capacitors (F)
rs1 = 0.2:0.05:0.4;           // Switch on-resistance during stage 1 (ohm)
rs2 = 0.2:0.05:0.4;           // Switch on-resistance during stage 2 (ohm)
CL  = 150e-9:1e-9:200e-9;     // Load Capacitor (F)
```

```
C_best= 68.00 nF
rs1_best= 0.30 ohm
rs2_best= 0.30 ohm
CL_best= 160.00 nF
```

Figure 3.20: System design results.

To verify if the obtained values allow the output voltage to reach the desired value with $V_i = 0.9$ V, a graphical plot was performed. The results are depicted in figure 3.21. The voltage is slightly above 2.5 V, which will allow some manoeuvrability in the closed-loop regulation.

3.2 Output regulation

As it was previously seen, in order to guarantee that the flying capacitors fully discharge each cycle, ϕ_2 can be kept constant. Therefore, it can be generated by a square wave oscillator. To generate the signal ϕ_1, a possible approach is to employ a classic PWM control. The basic control scheme is shown in figure 3.22.

The main basic operation is the following: the error between the desired voltage reference and the output voltage is amplified (K_3) and compared with a sawtooth wave. The result generates a

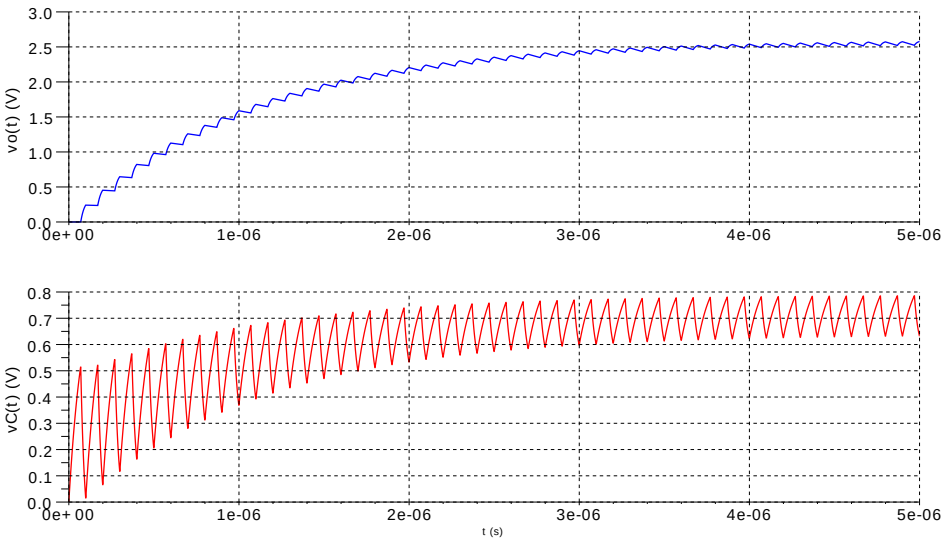

Figure 3.21: Output and flying capacitor voltage plot with the computed system parameters for $V_i = 0.9$ V.

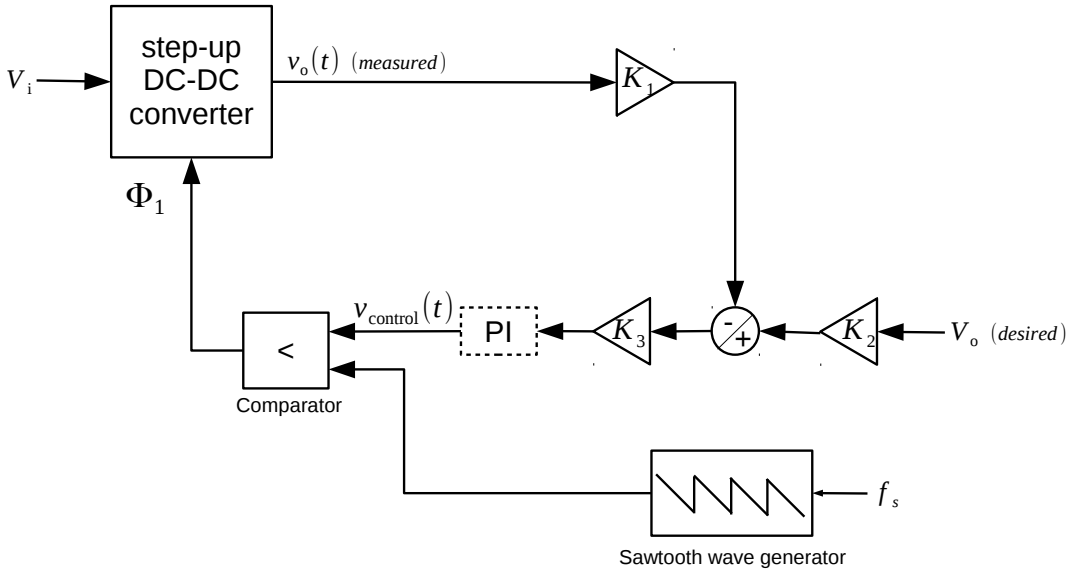

Figure 3.22: Closed-loop control scheme.

control signal with variable duty-cycle. If necessary, the error can be processed by a controller, usually a PI controller. The error can be determined using the actual voltage values or with attenuated voltage values (by making $K_1, K_2 < 1$), which are usually more convenient to process.

The sawtooth wave minimum voltage is 0 V and its maximum value is given by equation 3.27 [9].

$$V_{STW,max} = \frac{v_{Control}}{D_{\phi_1}} \tag{3.27}$$

In steady state $v_{Control} \simeq$ constant, but D_{ϕ_1} is only constant for a given V_i or I_o value. If one of them changes, a different D_{ϕ_1} is required. This phenomenon is best described by figure 3.23, which was plotted with data from the behavioural simulations and will be described in the next chapter. For higher I_o and lower V_i a larger D_{ϕ_1} is necessary. But as I_o decreases and V_i increases the required D_{ϕ_1} value decreases. Since the duty-cycle range variation is so large it may be difficult to achieve a good line and load regulation with this type of control.

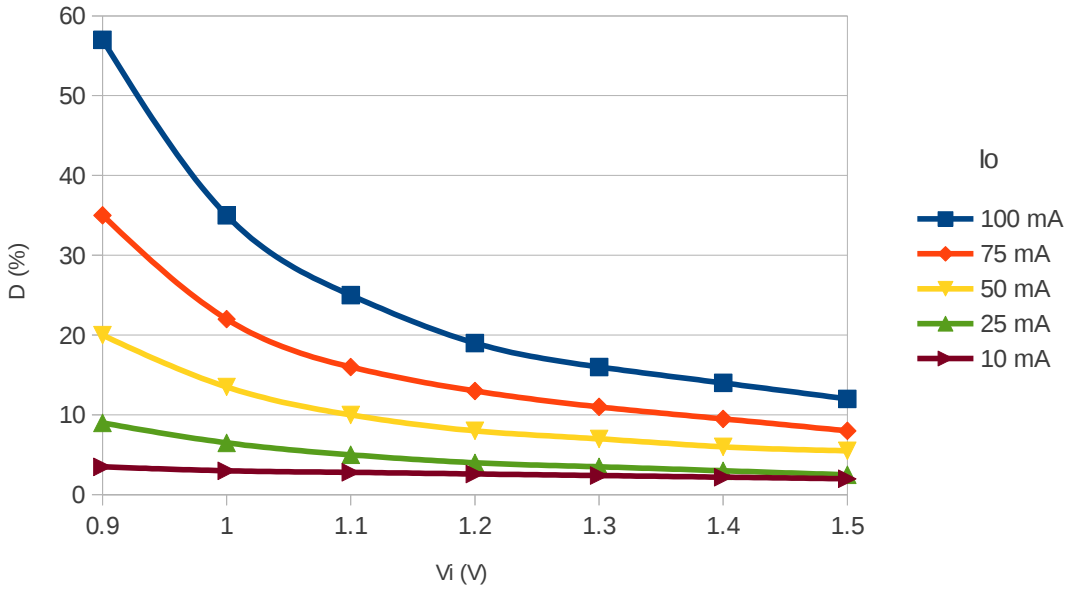

Figure 3.23: D_{ϕ_1} vs V_i for several I_o values.

A possible solution is to employ a variable voltage sawtooth wave generator, with a peak value depending on the input voltage. This way, it is possible to produce different duty-cycle values for the same $v_{control}$. An example is depicted in figure 3.24, where the effect of the amplitude variation in the duty-cycle value is clear.

In the beginning of the chapter it was stated that $D_{\phi_1} + D_{\phi_2} \leq 1$, but in reality the restriction between the control signals is given by

$$D_{\phi_1} + d_{dt1} + D_{\phi_2} + d_{dt2} = 1 \tag{3.28}$$

for $d_{dt1} \geq d_{dt2}$, where d_{dt1} and d_{dt2} are the duration of the dead time.

For a proper output regulation it is essential that the switch command signals do not overlap. If they have simultaneously, at any given instant, a high logic signal, some sections of the converter become short-circuited and undesirable or unpredictable behaviour may occur. So, when at a

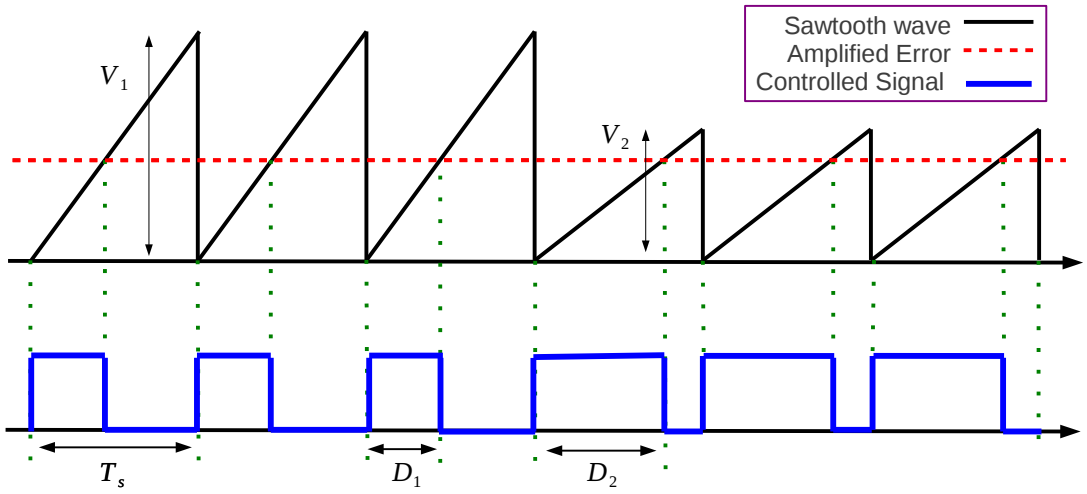

Figure 3.24: Variable voltage sawtooth wave generator output example

certain instant, both ϕ_1 and ϕ_2 are high, if a time delay (also called a dead time) is inserted between the two signals, this undesirable situations can be prevented. A possible way of generating dead time between the two signals is shown in figure 3.25 along with a time diagram.

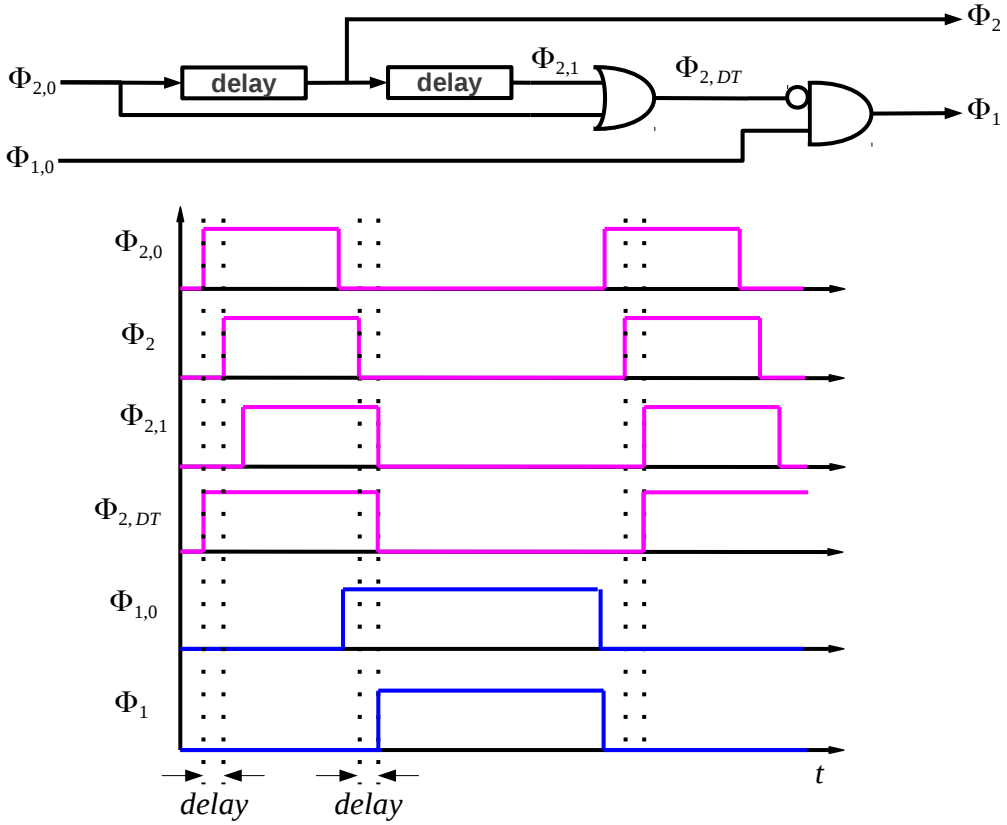

Figure 3.25: Dead time generator functional schematic and time diagram.

The original signals generated by the closed-loop regulation are called $\phi_{1,0}$ and $\phi_{2,0}$, respectively. $\phi_{2,0}$ is delayed twice and an OR operation between the original signal and the delayed signal is performed in order to ensure a minimum dead time before and after ϕ_2. The OR operation result, called $\phi_{2,DT}$ is then used to prevent ϕ_1 from being high when ϕ_2 is also high.

Chapter 4

Behavioural Simulations

In order to verify if the series-parallel switched capacitor converter, as well as the proposed regulation block met the basic requirements of the project, first a series of behavioural simulations were performed. They served as a mean of confirming if the deduced mathematical model was correct and were also useful to have an idea of certain values, such as the switch on-resistance, peak currents, flying capacitances magnitude, all important for later use in the design of the MOSFETs and other system components. The simulations were performed with Matlab®/Simulink® and the main libraries used were the Simulink and the Simscape™ library.

The converter circuit schematic used for all behavioural simulations with 3 flying capacitors is shown in figure 4.1.

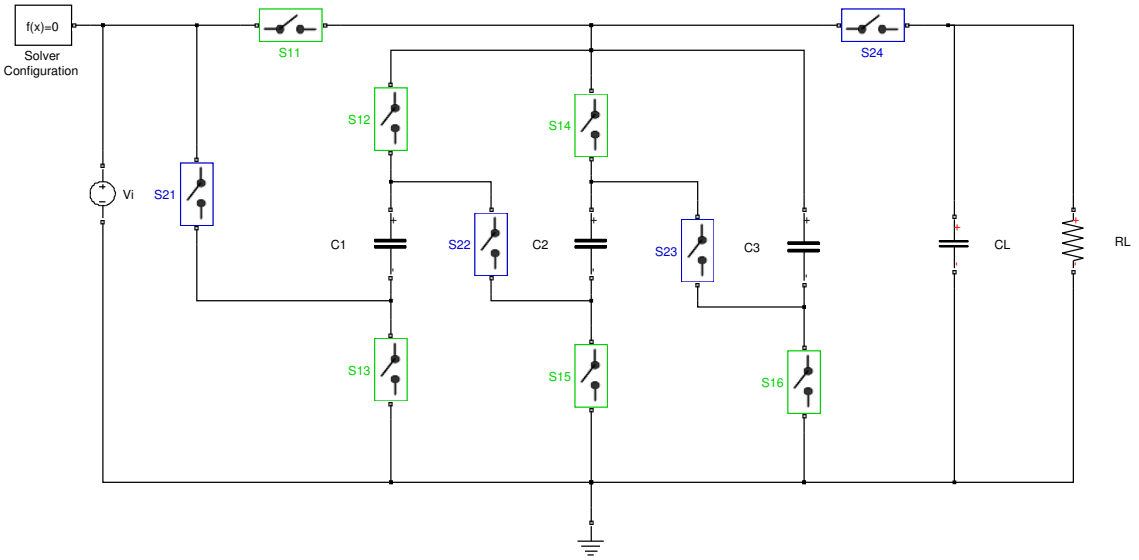

Figure 4.1: Converter circuit schematic with 3 flying capacitors.

4.1 Open-Loop simulations

4.1.1 Simulation with ideal switches

Since in this stage the design details are not particularly important, the simulations begun with ideal switches. Therefore, the on-resistance and off-conductance were considered very low:

$$Rs_{on} = 1 \text{ p}\Omega \tag{4.1}$$

$$Gs_{off} = 1 \text{ n}\Omega^{-1} \tag{4.2}$$

The switch subsystem of the ideal behavioural simulations is shown in figure 4.2. To achieve the desired output regulation, the green switches ($S_{1,i}|_{i\in[1,2n]}$) are controlled by the signal ϕ_1 and the blue switches ($S_{2,j}|_{j\in[1,n+1]}$) by the signal ϕ_2. These signals are generated by the regulation block. The open-loop regulation block consists of two square wave generators, as shown in figure 4.3.

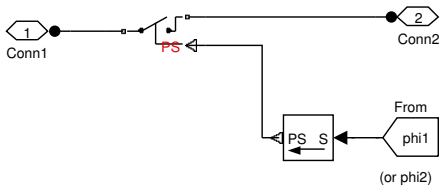

Figure 4.2: Ideal switch subsystem.

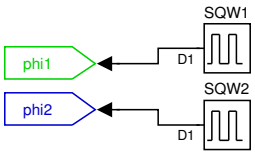

Figure 4.3: Open-loop regulation block.

4.1.1.1 Regulation block

SQW1 generates the control signal ϕ_1 and SQW2 generates ϕ_2. The main parameters used in each square wave generator block are specified in table 4.1.

Table 4.1: Open-loop square waves generators block parameters.

	SQW1	**SQW2**
Amplitude (V)	3	3
Period (s)	T_s	T_s
Duty-Cycle (%)	D_{ϕ_1}	D_{ϕ_2}
Phase Delay (s)	0	$\left(1 - \frac{D_{\phi_2}+d_{dt2}}{100}\right) T_s$

For this particular block, at the beginning of each period the square wave starts with the value defined in the *amplitude* field and then, when the time defined by the duty-cycle is over, is set to 0 V until the end of the period. Since at the beginning of each period ϕ_2 has an amplitude of 0 V, SQW2 needs to have a *phase delay* field > 0. If not, the signals ϕ_1 and ϕ_2 will overlap.

It was seen in section 3.2 that $D_{\phi_1} + d_{dt1} + D_{\phi_2} + d_{dt2} = 1$ and $d_{dt1} \geq d_{dt2}$, where d_{dt1} and d_{dt2} are the dead time duration between the control signals ϕ_1 and ϕ_2. The specific value of d_{dt2} is

not very important, as long as it is kept larger than the simulation time step, to ensure a better performance, and kept much smaller than the minimum duty-cycle of ϕ_2.

4.1.1.2 Simulation results

The ideal open-loop simulations were performed with the values, chosen for practical purposes, indicated in table 4.2 and the simulation results are shown in figure 4.4.

Table 4.2: Open-loop simulation with ideal switches: parameters.

fs (MHz)	100
$C_{1,2,3}$ (nF)	50
C_L (nF)	300
R_L (Ω)	25
D_{ϕ_1} (%)	50
D_{ϕ_2} (%)	45

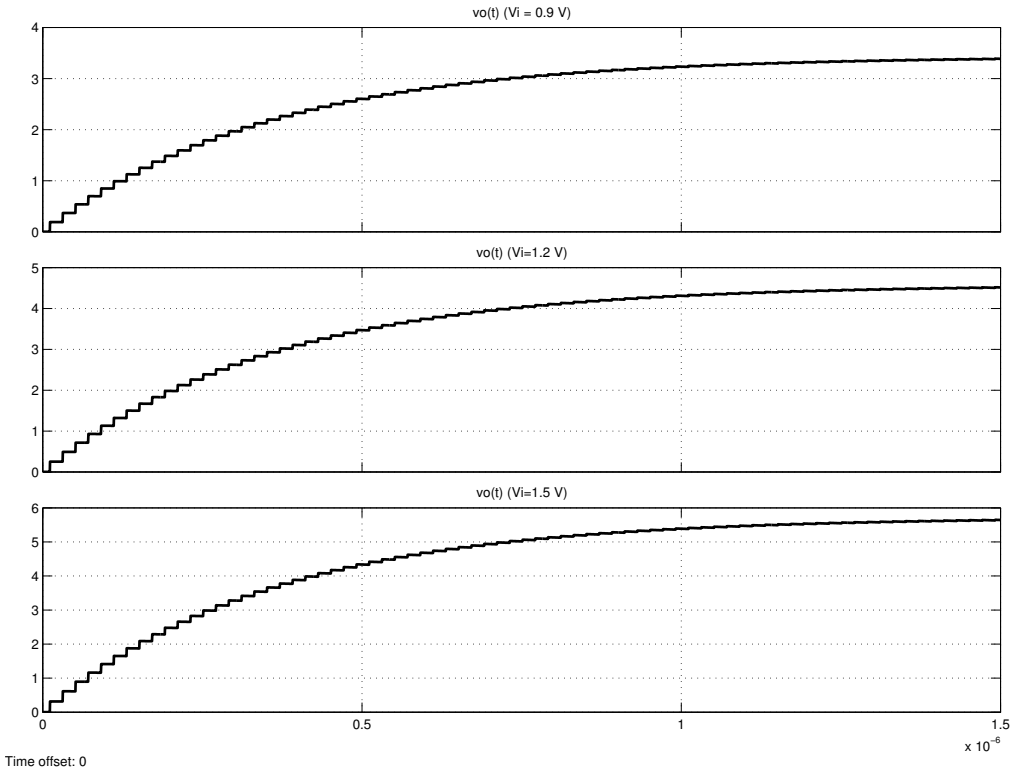

Figure 4.4: Open-loop simulation results with ideal switches: Output voltage for $V_i = \{0.9;1.2;1.5\}$ V.

For $V_i = \{0.9;1.2;1.5\}$, the steady state values are very close to the ideal ones, which are given by $0.9 \times 4 = 3.6$, $1.2 \times 4 = 4.8$ and $1.5 \times 4 = 6$, respectively.

4.1.2 Simulation with more realistic switch models

In order to approximate the voltage controlled resistor model of the MOSFET, the ideal switches were replaced by sightly more realistic models. The off-conductance remained the same as equation 4.2, but the on-resistance considered for the stage 1 and 2 switches are given by equations 4.3 and 4.4, respectively.

$$R_{Son} = r_{S1} \text{ or } \frac{r_{S1}}{2} \tag{4.3}$$

$$R_{Son} = r_{S2} \tag{4.4}$$

The simulation performed employed the same control scheme of that presented in the previous section, but with the values determined in chapter 3, subsection 3.1.4, which are presented in table 4.3. The simulation results are shown in figure 4.5.

Table 4.3: Open-loop simulation with more realistic switches: parameters.

f_s (MHz)	10
$C_{1,2,3}$ (nF)	68
C_L (nF)	140
R_L (Ω)	25
r_{S1} (Ω)	0.3
r_{S2} (Ω)	0.3
D_{ϕ_1} (%)	68
D_{ϕ_2} (%)	30

For $V_i = 0.9$ V, the simulation results are very similar to the expected theoretical results depicted in figure 3.21. For $V_i \geq 0.9$ V the steady state output voltage is always greater than 2.5 V. Which means that with a good regulation system, the output voltage can be kept around 2.5 V.

4.1.2.1 Mathematical model validation

After converter's mathematical model deduction described in chapter 3, it became necessary to validate the obtained equations. So, in the next subsection two scenarios are presented, which illustrate the resemblance between the simulation results and the results obtained through the mathematical model. The graphical plots were made with the source code presented in appendix C.

The parameters used in the first example are listed in table 4.4. The theoretical results are shown in figure 4.6 and the simulation results in figure 4.7. The parameters used in the second example are listed in table 4.5. The theoretical results are shown in figure 4.8 and the simulation results in figure 4.9. In both examples the conclusions are very similar. In each case, for both flying capacitors and output voltage, the same steady state value is achieved. The theoretical response and settling times are also very similar to the ones obtained through simulation. Thus, the results of the theoretical model match with a great level of accuracy the open-loop simulation results with semi-ideal switches. Not only for the specific requirements of the current project, but also

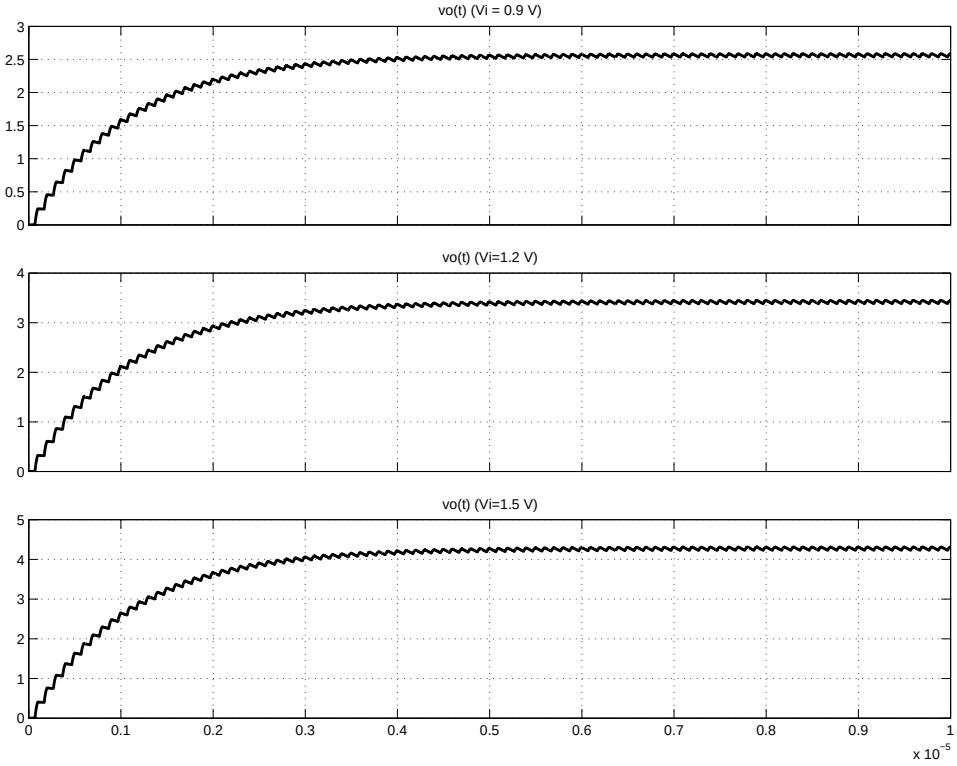

Figure 4.5: Open-loop simulation results with more realistic switches: Output voltage for $V_i = \{0.9; 1.2; 1.5\}$.

for different scenarios, which means that the deduced model can be used to design other step-up series-parallel switched-capacitor converters with completely different requirements.

Table 4.4: Example 1: parameters

f_s (MHz)	50
V_i (V)	2
n	6
C (nF)	5
C_L (nF)	20
R_L (Ω)	1000
r_{S1} (Ω)	1
r_{S2} (Ω)	1
D_{ϕ_1} (%)	50
D_{ϕ_2} (%)	48

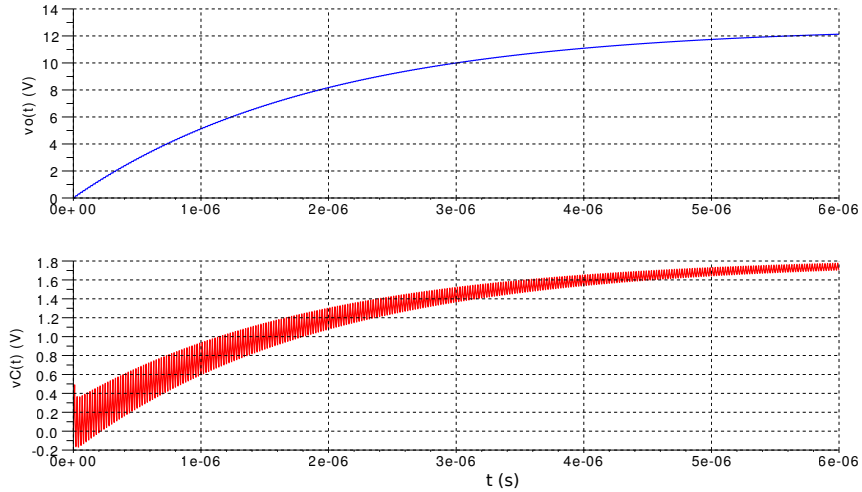

Figure 4.6: Example 1: theoretical results.

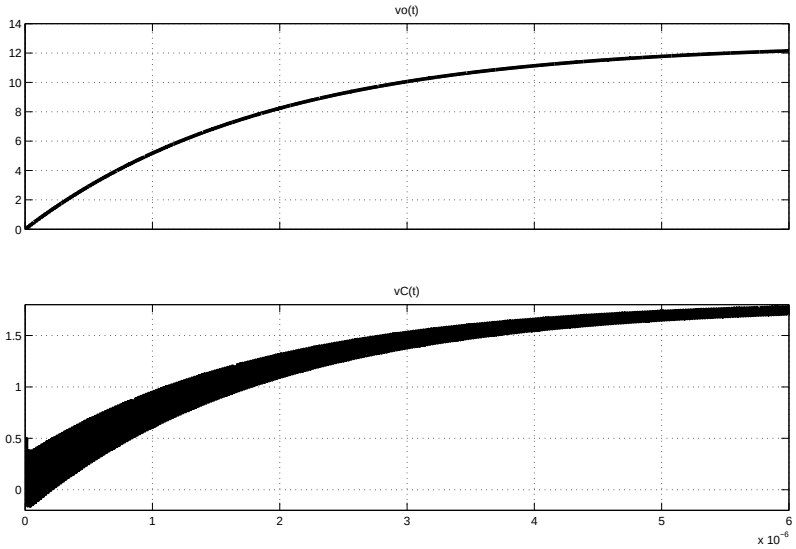

Figure 4.7: Example 1: simulations results.

Table 4.5: Example 2: parameters.

f_s (MHz)	1
V_i (V)	0.2
n	4
C (nF)	50
C_L (nF)	100
R_L (Ω)	10000
r_{S1} (Ω)	1.5
r_{S2} (Ω)	1.5
D_{ϕ_1} (%)	60
D_{ϕ_2} (%)	38

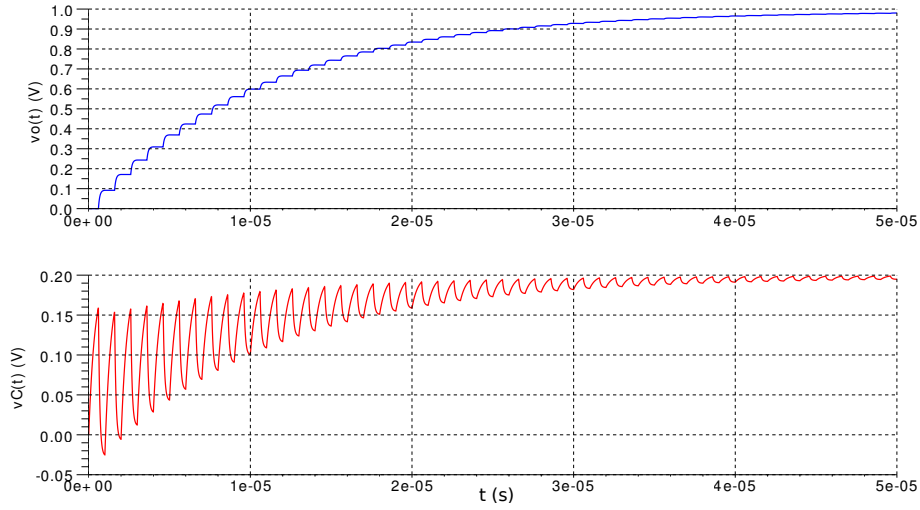

Figure 4.8: Example 2: theoretical results.

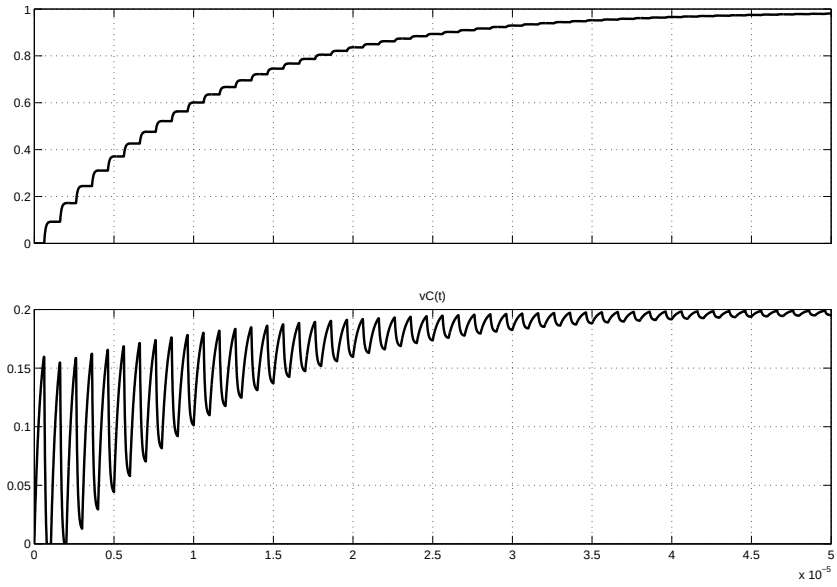

Figure 4.9: Example 2: simulations results.

4.2 Closed-loop simulations

After the open-loop simulations were completed, ideal closed-loop simulations were performed. Only the results of the closed-loop simulations made with the non-ideal switches will be shown, since the final overall results were very similar and the simulations with ideal switches will add no other relevant information.

The main challenge was to guarantee a constant output regulation, since the input voltage can vary by specification between 1.2 ± 0.3 V. So, the system was designed around the minimum input voltage. The electrical component values had to be chosen in order to ensure that the output voltage reaches 2.5 V when the input voltage is 0.9 V, which was somewhat inconvenient, since

considerably larger capacitor values and a smaller on-resistance were obtained, compared to the values found if the system was designed for the nominal input voltage.

4.2.1 Regulation block

The closed-loop simulations were performed with the values indicated in table 4.6. These values, as indicated in chapter 3 subsection 3.1.4, acquired through the parameter extraction program based on the mathematical model of the converter, represent the maximum on-resistance and the minimum flying capacitance that allows the output to reach a mean value of 2.5 V for the minimum input voltage (and higher values for higher input voltages) in open-loop.

Table 4.6: Closed-loop simulations: parameters.

f_s (MHz)	10
$C_{1,2,3}$ (nF)	68
C_L (nF)	140
R_L (Ω)	25
r_{S1} (Ω)	0.3
r_{S2} (Ω)	0.3
D_{ϕ_2} (%)	30

The proposed regulation block is shown in figure 4.10. It is very similar to the regulation scheme previously presented in figure 3.22 in chapter 3 section 3.2, where the error between the reference voltage $VoRef$ and the output voltage V_o is calculated, then amplified. In this particular case the error had to be processed by a PI controller, to attenuate the abrupt voltage swings during the steady state. The output of the PI controller, $v_{control}$, is then compared with a sawtooth wave, and the signal $\phi_{1,0}$ is generated. Then, it is processed by the dead time generator block, to avoid signal overlap, and ϕ_1 is generated. ϕ_2 is constant and has a pre-established duty-cycle of 30 %. The basic operation principle of the time generator block was also presented in subsection 3.2. The implementation based on the theory previously described is shown in figure 4.11.

Once again, the value of the constants *delay1* and *delay2* are not particularly important, as long as they are kept higher than the simulation time step and smaller than the minimum duty-cycle to allow a better performance. In this simulation stage, the variable voltage sawtooth wave generator was achieved with a simple switched RC circuit, as shown in figure 4.12.

The operation principle is very simple. When the switch S_1 is on and S_2 is off, the capacitor charges through the resistor R_1. When S_1 is off and S_2 is on, the capacitor is disconnected from the source and discharges trough the resistor R_2. The pulse generator block is responsible for controlling the switches on duration and assuring a small dead time between the two command signals. The main parameters used in this block are listed in table 4.7.

An output sample of the variable voltage sawtooth generator is depicted in figure 4.13.

The result shown in figure 4.13 is very similar to the one presented in the theoretical analysis of figure 3.24 in chapter 3, section 3.2. The amplitude of the sawtooth wave changes with V_i and for higher input voltages, the duty-cycle of ϕ_1 decreases, as expected.

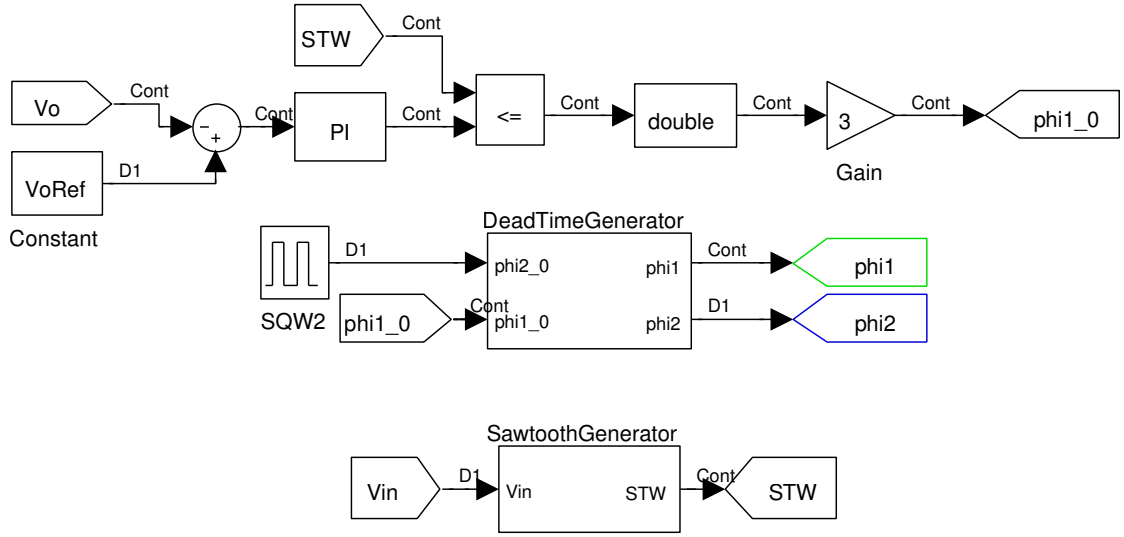

Figure 4.10: Regulation block overview.

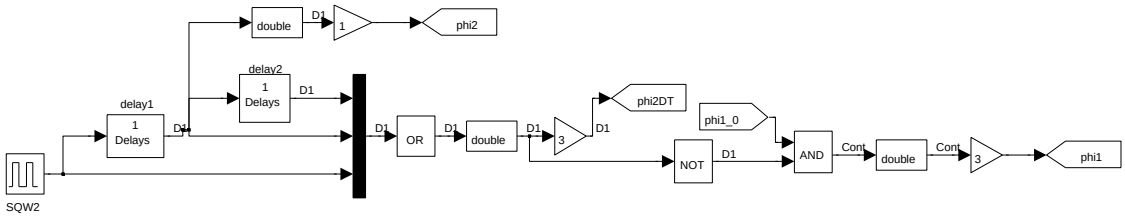

Figure 4.11: Dead time generator block.

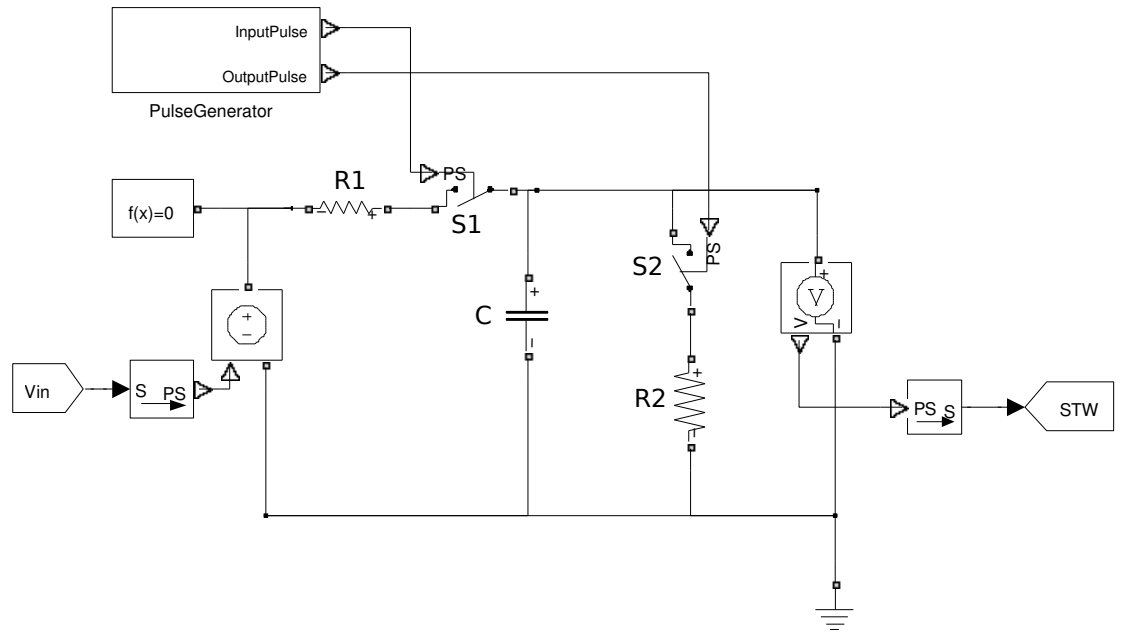

Figure 4.12: Variable sawtooth wave generator block.

Table 4.7: Sawtooth wave generator: parameters.

R_1 (Ω)	50
R_2 (Ω)	1
C (nF)	1
D (%)	5

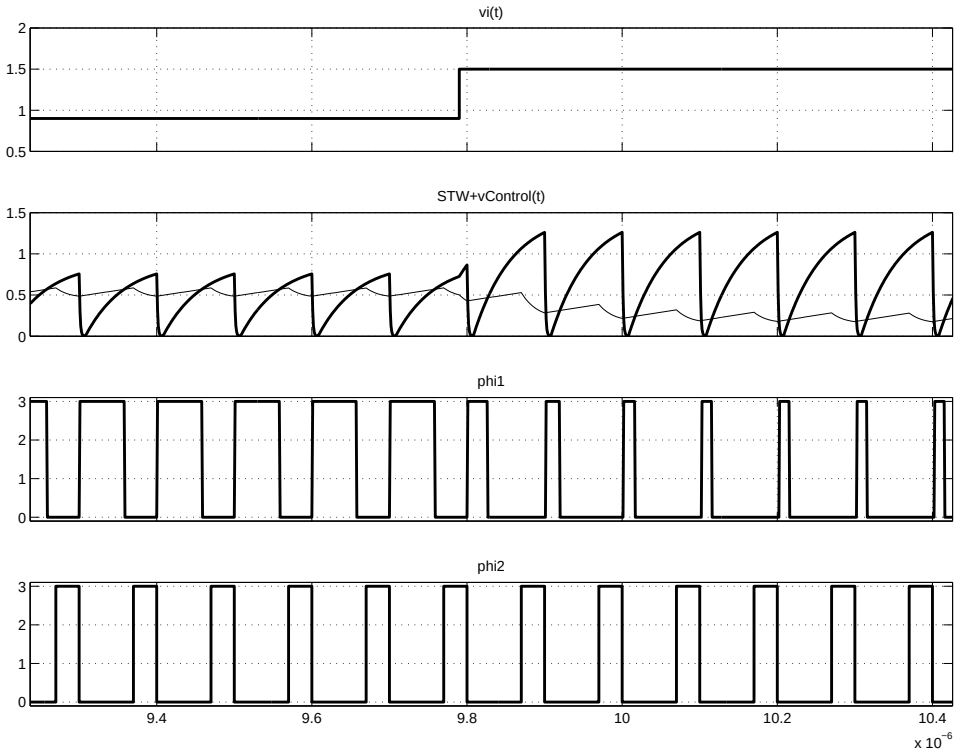

Figure 4.13: Variable sawtooth wave generator output example.

4.2.2 Simulation results

In order to test the regulation capability of the proposed regulation block, variable input voltage and variable load current tests were performed. The results for the variable input voltage are shown in figure 4.14, where V_i was stepped from 1.2 to 0.9 and then to 1.5 V in order to test the system for the nominal input voltage and for the bounds of the remaining allowed range, approximately maintaining a constant load current of 100 mA.

Despite of some undershoot when transitioning from 1.2 to 0.9 V and some overshoot when stepping from 0.9 to 1.5 V, the output voltage eventually stabilizes around 2.5 V. Next, figure 4.15 shows the results of the load variation tests made for $V_i = 1.2$ V. The converter was submitted to the nominal load (100 mA), then a smaller load of 10 mA, 50 % of the load and finally 150 % of the nominal load.

This figure shows that, despite of the good regulation achieved, the output voltage ripple increases with I_o. Having a closer look to the time frame, it is visible that when submitted to load variations, the output takes longer to stabilize than it would take if submitted to input voltage

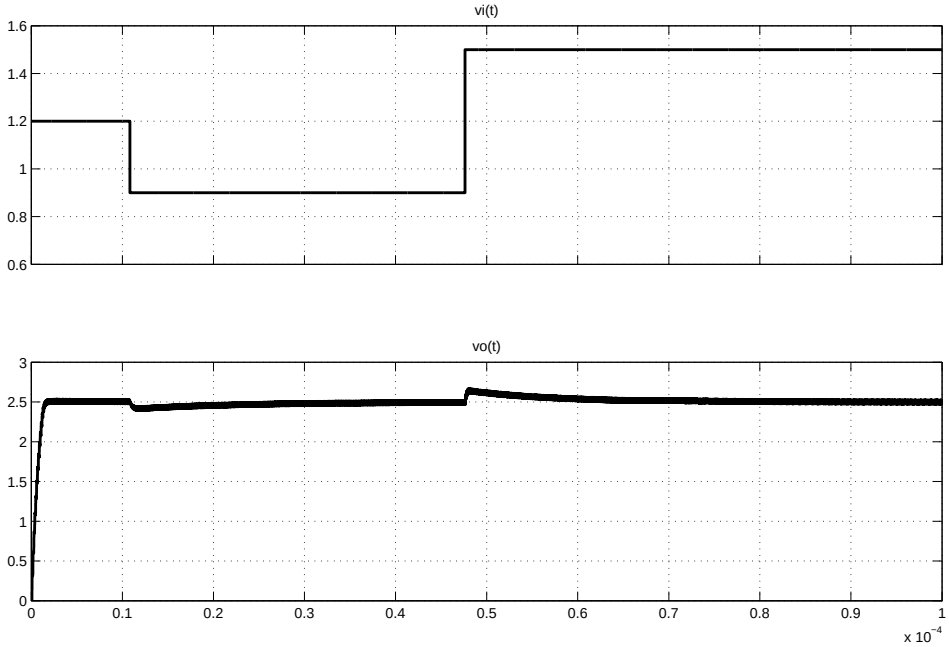

Figure 4.14: Output voltage for variable input voltage with constant load (V).

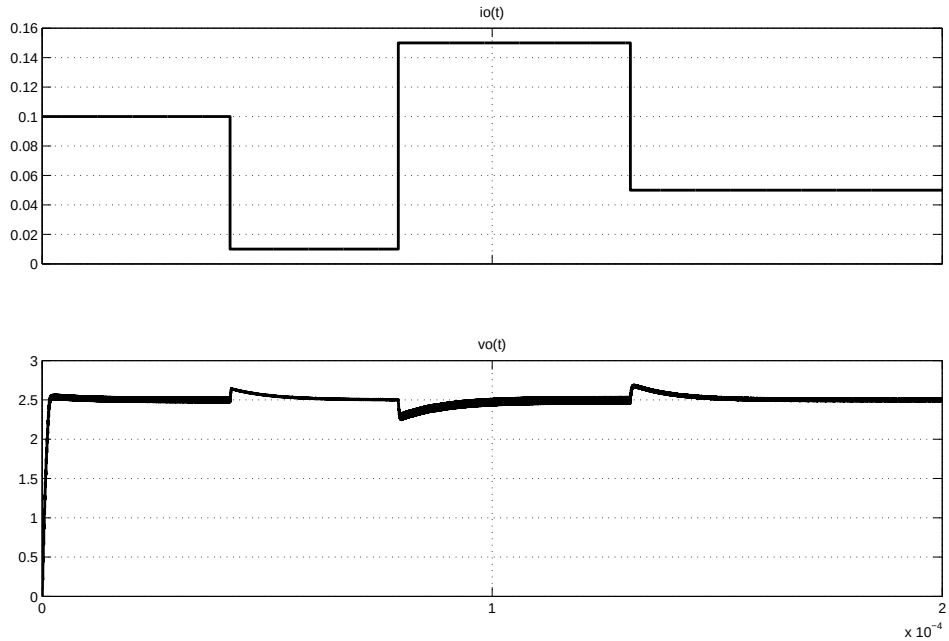

Figure 4.15: Output voltage for $V_i = 1.2$ V with variable load current (V).

variations.

These evaluations where not extensive, and did not have as a main purpose to verify the limits of the converter and the regulation block, but only to see if they met the basic requirements of the project. From figure 4.15 it was arrived to the conclusion that the converter withstands some level of load variations and can operate with a very low load, but when the current load increases, the

output ripple also increases, which can be attenuated by increasing the value of C_L. When line variations occur, the output voltage has some under and overshoots, but do not appear significant and the output voltage always converges to the reference value with the same approximate level of ripple.

Now that it has been proven that the converter topology and the regulation block meet the basic requirements of the project, the next step is to design the MOSFETs, capacitors and the regulation block with more realistic models, down to the transistor level, and make a more extensive study of the operation and limitations of these two system elements.

Chapter 5

Simulations With More Realistic Models

The software used to perform the simulations with more realistic models was Cadence. The first step was to extract the necessary process parameters of 0.35 μm CMOS technology to properly design the basic system components. Replicate the behavioural simulations described in chapter 4, substituting the ideal switches with MOSFETs. Then, gradually replace the remaining sections of the system with more realistic models, making the necessary simulations to ensure that the system still behaves as desired.

Some components, such as operational amplifiers, were not replaced by the transistor-level models and were kept with the functional models. An operational amplifier model was developed, but when inserted in the system some complications appeared, such as an undesired offset in the output voltage of the amplifier. Thus, it was decided to keep the functional models of these elements.

5.1 MOSFETs design

In chapter 3 subsection 3.1.4 was stated that the MOSFETs maximum on-resistance is 300 mΩ. In chapter 2 subsection 2.2.2 was seen that in the triode region the on-resistance of a MOSFET is given by equation 5.1.

$$r_{on} = \frac{L}{W}\frac{1}{k_{n,p}(|v_{GS}| - |V_{Tn,p}|)} \tag{5.1}$$

The previous equation can be rewritten as

$$\frac{W}{L} = \frac{1}{k_{n,p}r_{on}}\frac{1}{|v_{GS}| - |V_{Tn,p}|} \tag{5.2}$$

For this converter topology, the v_{GS} voltages of the MOSFETs are not constant throughout its operation and change further with line variations. So, the transistors have to be designed considering the worst case scenario. Analysing equation 5.2, considering L, r_{on}, $k_{n,p}$ and $V_{Tn,p}$ constants, it can be concluded that W increases when $|v_{GS}|$ decreases.

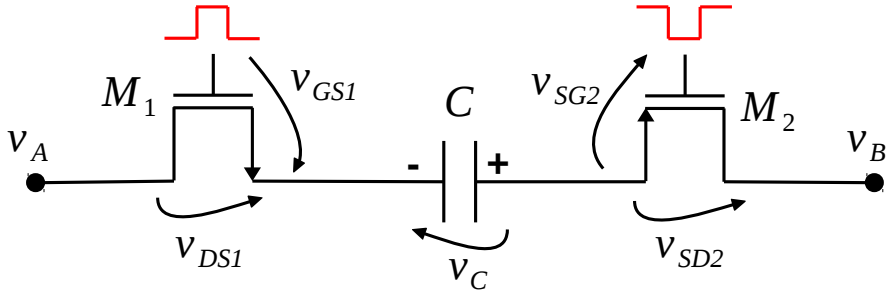

Figure 5.1: Node voltage analysis.

Using figure 5.1 as a reference and inspecting the converter node voltages during the triode operation, for M_1 the gate-source voltage drop is smaller for lower v_A values. For instance,

$$v_{GS} = vdd - (v_A - v_{DS1}) \tag{5.3}$$

Ignoring the MOSFETs drain-source voltage drop, for simplicity,

$$v_{GS} = vdd - v_A = 3 - 0.9 = 2.1V \text{ and } v_{GS} = 3 - 1.5 = 1.5V \tag{5.4}$$

For M_2 a similar analysis can be done.

$$v_{SG} = |v_{GS}| = v_A + v_C - 0 = 0.9 + v_C \text{ and } v_{SG} = |v_{GS}| = 1.5 + v_C \tag{5.5}$$

For M_1, the gate-source voltage drop is lower when considering v_C=0 V. Thus, for the NMOS $|v_{GS}|$ is minimum when $V_i = 1.5$ V and for the PMOS when $V_i = 0.9$ V, considering the flying capacitors discharged and ignoring the influence of the MOSFETs drain-source voltage drop.

With that in mind, a computational program was developed to compute the transistors channel width, based on an iterative process for a more precise design. Since the MOSFETs have large dimensions, it was considered L=0.35 μm for all the transistors. The design of the converter MOSFETs was more careful and the process parameters for this situation were not assumed constant for all W range, due to the on-resistance requirements. If the on-resistance of the converter MOSFETs is larger than the theoretical values, the flying capacitors may not charge and consequently the output voltage may not reach the desired value.

The source code is in appendix C, section C.3 and the flowchart is presented in figure 5.2. The basic principle behind the MOSFET design is the following: the process parameters are stored in arrays. The program begins with a pointer in the beginning of each vector. For every $k_{n,p}/V_{Tn,p}$ pair, and corresponding theoretical length W, a new length and MOSFET number is calculated, which equivalent on-resistance is equal or very close to the desired value. The length is calculated

with resort to equation 5.2. The number of transistors starts with 1. If the computed length is larger than the maximum length, a new MOSFET is added in parallel. The on-resistance of each transistor is increased and the new length value computed. When the length is smaller than the maximum values, the error between the computed length and the theoretical length is calculated. If the error is smaller than the previous one, the current length and number of transistors are stored. If not, the process begins again until all $k_{n,p}/V_{Tn,p}$ pairs are used. The final length and MOSFET number corresponds to the result with the smallest error.

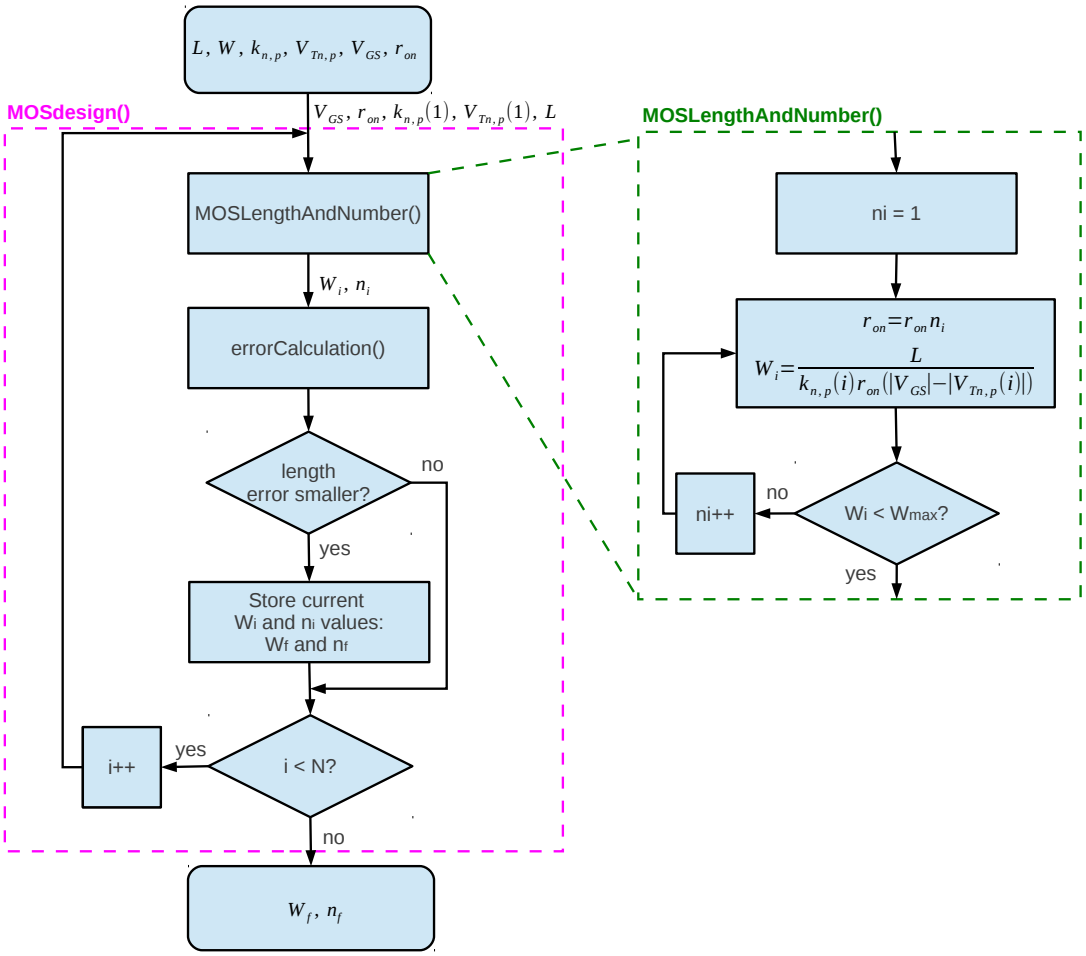

Figure 5.2: Converter MOSFET design flowchart.

When choosing what type of MOSFET to employ, priority was given to PMOS transistors due to the radiation features. However, the low input voltage requirements, specially for voltages smaller than 1 V, prevented the employment of this type of MOSFETs in certain circuit areas, since the condition $v_{DS} > v_{GS} - V_T$ could not always be met. So, the MOSFETs closest to the input were implemented with NMOS. Also, the ones with the source terminal connected to the ground were implemented with NMOS transistors, since during conduction an approximately constant gate-source voltage, independent of node voltage swings and only dependent of Vdd, is assured. An

overview of the converter is shown in figure 5.3. The results of the MOSFETs design are shown in figure 5.4.

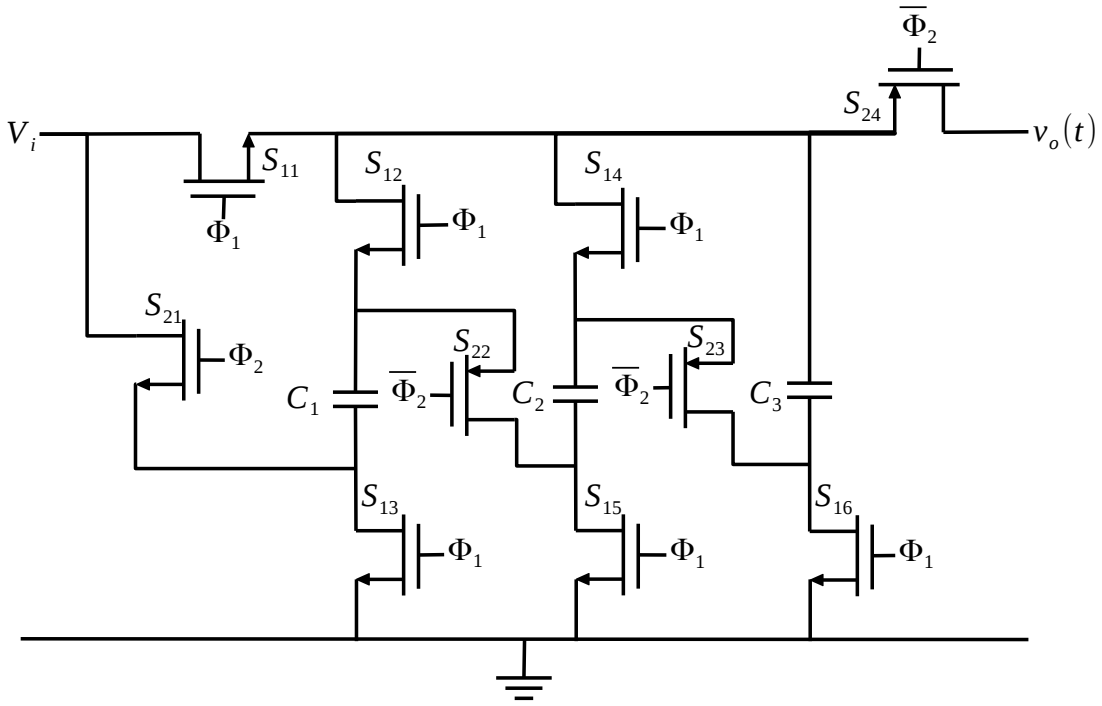

Figure 5.3: Converter overview after the MOSFETs design.

```
Stage 1

S11N
number = 2
W= 6891.53 um
theoretical W= 7000.00 um

S12N and S14N
number = 3
W= 4873.91 um
theoretical W= 5000.00 um

S13N and S15N
number = 2
W= 5691.06 um
theoretical W= 6000.00 um

S16N
number = 1
W= 5691.06 um
theoretical W= 6000.00 um
```

```
Stage 2

S21N
number = 2
W= 6891.53 um
theoretical W= 7000.00 um

S22P, S23P and S24P
number = 4
W= 5732.44 um
theoretical W= 6000.00 um
```

Figure 5.4: Converter MOSFET design results.

5.2 System design

The main parameters used to design the system are listed in table 5.1. Initially, a theoretical value of $C_L = 160$ nF, computed in chapter subsection 3.1.4, was employed. However, as expected, the open-loop regulation was a bit challenging and some issues emerged during the closed-loop regulation design. A solution using a PI controller was employed, but proved to be more effective the increase of the output capacitor value. Since the output capacitor cannot be implemented on-chip due to its large capacitance value and since the difference in size between a 160 nF and a 300 nF external capacitor is not very significant, a capacitance increase may not be a considerable disadvantage. Besides, a larger capacitor decreases the output voltage ripple.

Table 5.1: Main system parameters.

Parameter	**Value**	**units**
f_s	10	MHz
$C_{1,2,3}$	68	nF
C_L	300	nF
R_L	25	Ω

5.2.1 Converter

An overview of the converter is shown in figure 5.5. The parameters of each MOSFET are depicted in table 5.2. The flying and output capacitors have to be implemented off-chip due to their large capacitance value.

Table 5.2: Converter MOSFET main parameters.

Switch	**Type**	**W (μm)**	**Quantity**
S_{11}	NMOS	6890	2
S_{12}, S_{14}	NMOS	4870	3
S_{13}, S_{15}	NMOS	5690	2
S_{16}	NMOS	5690	1
S_{21}	NMOS	6890	1
S_{22}, S_{23}, S_{24}	PMOS	5700	4

The converter schematic is essentially the same as the one shown in figure 5.3, with the number of MOSFETs indicated in table 5.2 connected in parallel. The dimensions are not exactly the same as the ones computed and shown in figure 5.4 since the software itself rounded up the values.

5.2.2 Closed-loop control

The closed-loop regulation was achieved with the circuit depicted in figure 5.6. The operation principle is the same as described in 3 subsection 3.2.

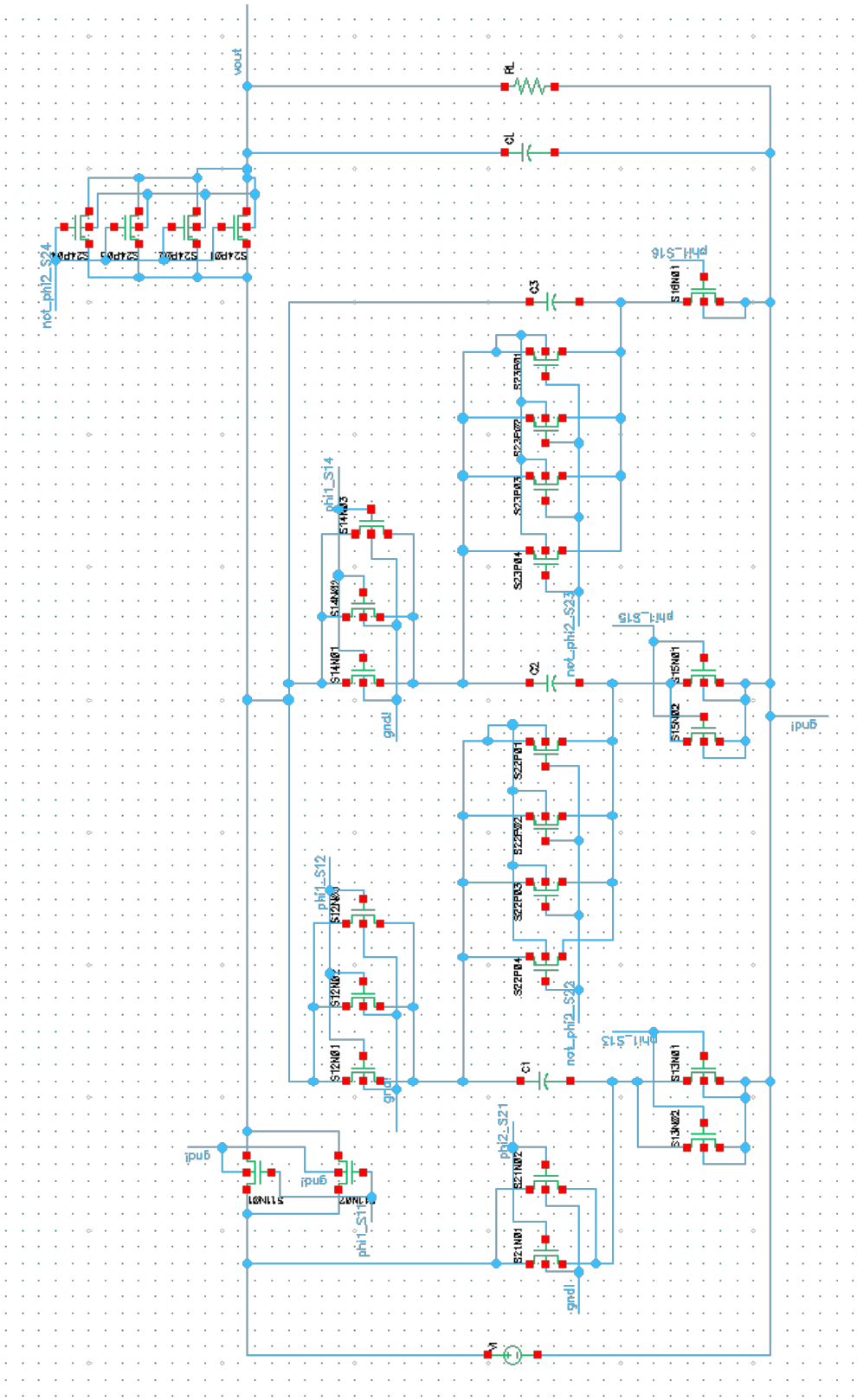

Figure 5.5: Converter circuit schematic.

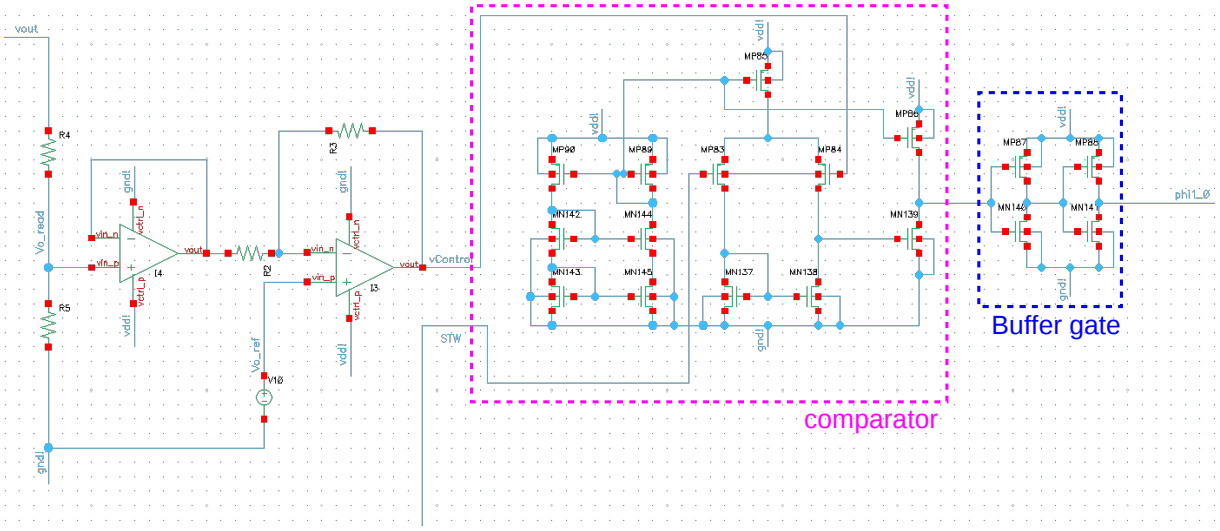

Figure 5.6: Closed-loop control schematic.

The voltage reference V_{oRef} was set to 300 mV. Another value could have been chosen, since the desired output voltage is 2.5 V, R_4 and R_5 are given by

$$
\begin{aligned}
V_{oRef} &= \frac{R_5}{R_4 + R_5} V_o \\
\Leftrightarrow R_4 &= \frac{V_o - V_{oRef}}{V_{oRef}} R_5 \\
\Leftrightarrow R_4 &= \frac{2.5 - 0.3}{0.3} R_5 \\
\Leftrightarrow R_4 &\backsimeq 7.33 R_5
\end{aligned}
$$

Setting $R_5 = 5$ kΩ results in $R_4 \backsimeq 36.666$ kΩ. At the voltage divider output, a buffer was used in order to assure the same approximate current value in both resistors R_4 and R_5 and to boost the current flowing in resistor R_2. Otherwise the operational amplifier I3 would not properly operate. This element simultaneously calculates the error between the current output voltage and the reference voltage and amplifies it. The internal gain was set to 10M, but the gain imposed by the external loop was adjusted manually. The gain was adjusted in order to have the desired steady-state duty-cycle value for ϕ_1 when $V_i = 1.2$ V and $I_o = 100$ mA, that allowed the output to reach 2.5 V with less than 1 % of voltage ripple.

As stated before, it was found easier to increase the output capacitor value to obtain a more stable $v_{Control}$ signal, then employ a PI controller. Both solutions were tried. In addition to a difficult tuning process that had to be redone whenever the input voltage changed (despite of the variable voltage sawtooth wave), the capacitor value was too large to be implemented on-chip, and due to precision issues the resistor would also have to be implemented off-chip. So, the increase of the output capacitor to 300 nF solved the problem without adding any extra external components

to the system.

The output voltage of the operational amplifier I3, considering that $R_3 >> R_2$, is given by

$$v_{Control}(t) \simeq \frac{R_3}{R_2}(V_{oRef} - v_{oRead}(t)) \tag{5.6}$$

The necessary gain was determined experimentally. In order to generate ϕ_1 with an appropriate duty-cycle that allows a proper output regulation for $V_i = 1.2$ V, the amplifier needs to have a gain around 125. With that information, the resistors R_3 and R_4 were designed as follows.

$$R_3 = 125R_2 \tag{5.7}$$

Setting $R_3 = 10$ kΩ, $R_2 = 80$ Ω. The system was designed around $V_i = 1.2$ V and not for $V_i = 0.9$ V as before, since with the variable sawtooth generator, the regulation block can be designed around a central point, allowing a certain degree of manoeuvrability when some parameters, such as input voltage or load current are changed.

In essence, the amplified error signal, called $v_{Control}$ is compared with the sawtooth wave generating $\phi_{1,0}$. All resistors should be implemented off-chip, since a significant deviation in resistance values can change considerably the control operation. A summary of all main results obtained is presented in table 5.3.

Table 5.3: Control circuit: main parameters.

Component	**Value**	**Units**
g3	10M	-
g4	10M	-
R2	80	Ω
R3	10k	Ω
R4	36.666k	Ω
R5	5k	Ω

5.2.2.1 Comparator

The comparator shown in figure 5.6, based on a two-stage amplifier model, was designed for a reference current of 10 μA, produced by a cascode current source. In order to assure a current flow with the same magnitude of the reference current, MP85 was set with the same size of MP89 and MP90. To minimize any possible output voltage offset, MN139 was defined with a W/L ratio twice the value of MN137 and MN138, also assuring that the current flowing in those transistors is half of the reference current. In the second stage, in order for the converter to have enough output current drive capability, MP86 was set with a size three times of MP85, making the flowing current in this stage three times larger than the reference current. A summary of the used values is depicted in table 5.4.

At the output of the comparator there was placed a buffer gate in order to increase the output current drive capability of the comparator, but mainly to improve the "shape" of the output square

Table 5.4: Comparator parameters.

Component	W	L	Units
MP85, MP89, MP90	1	1	μm
MN86	3	1	μm
MN144, MN142	4	1	μm
MN145, MN143	10	1	μm
MP83, MP84	10	0.35	μm
MN137, MN138	2	0.35	μm
MN139	4	0.35	μm

wave, improving the quality of the digital signal produced. This approach was used several times along the project. Unless stated other wise, the dimensions of each inverter in a buffer gate with two inverters are indicated in table 5.5.

Table 5.5: Standard buffer gate parameters (per inverter).

Component	W	L	Units
PMOS	10	1	μm
NMOS	5	1	μm

5.2.3 Variable sawtooth wave generator

The variable sawtooth generator was achieved employing the circuit shown in figure 5.7. It generates a current proportional to the input voltage which charges up the capacitor C_{S1} with a voltage dependent of the input. It is based on the current mirror principle. The current that charges the capacitor has the same value of the current that flows through resistor R_1. All MOSFETs, except MN0 and MN2, operate in the saturation region.

It was designed to generate a sawtooth wave with an amplitude of 1 V when the input voltage is 1.2 V with a rise time of 95 ns and a fall time of 5 ns. The previous parameters were pre-established since not all variables can or need to be calculated and can be set in the beginning of the design to simplify the analysis. The system was designed for 1.2 V and then tested for the remaining input voltages.

The C_{S1} capacitor was set with a value of 2.5 pF in order to be implemented on-chip. Then, the necessary current to charge the capacitor was determined.

$$i_C = C_{S1}\frac{\Delta V}{\Delta t} = 2.5p\frac{1}{95n} \simeq 26.316\mu A$$

To obtain the value of R_1, it is necessary to know the voltage drop across its terminals. So, the more positive terminal of the resistor was assumed to be at V_{R+} = 0.1 V. Therefore,

$$R_1 = \frac{0.1}{26.316\mu} \simeq 3800\Omega$$

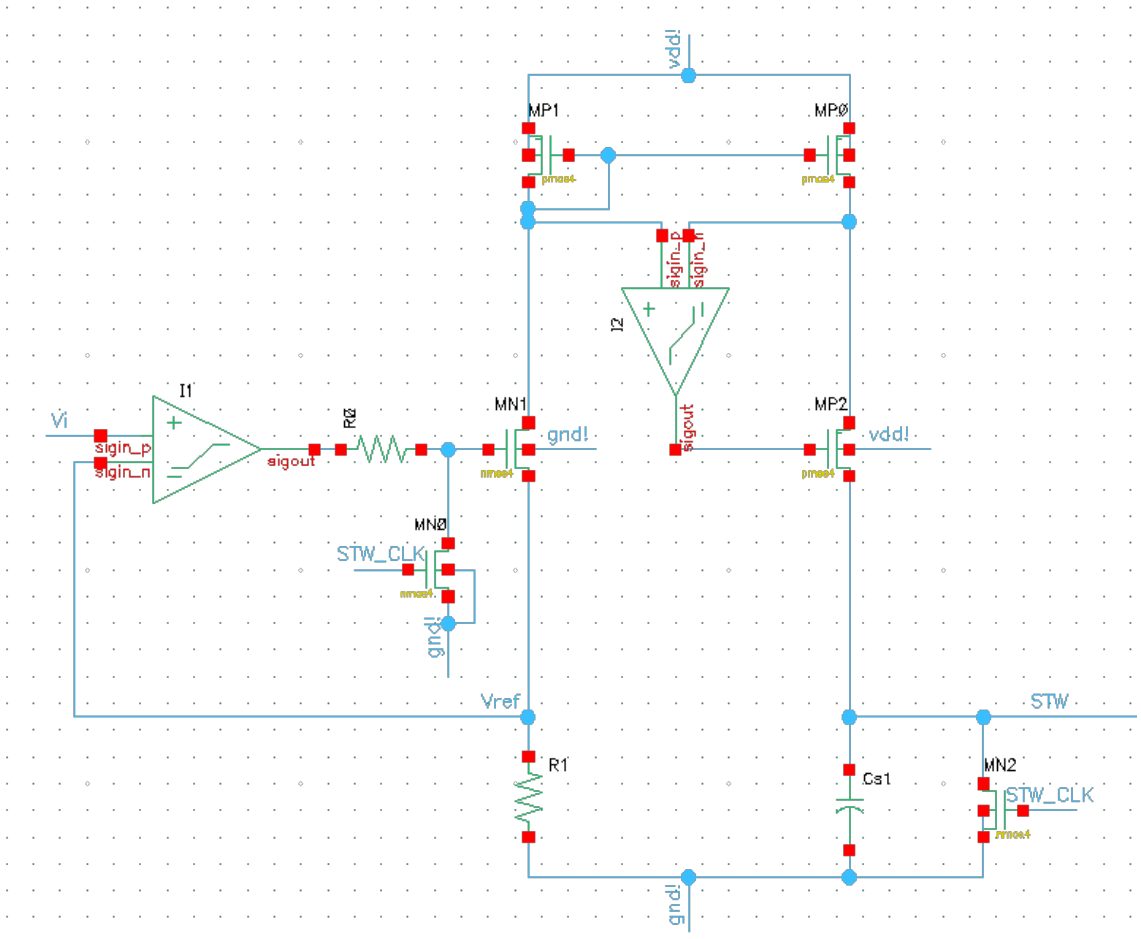

Figure 5.7: Variable sawtooth generator schematic.

R_1 has to be implemented off-chip, since MOS resistors have a tolerance around 30 % and a variation of that magnitude in the resistance value considerably changes the flowing current. External resistors have much smaller tolerances and can guarantee a more stable value during their operation.

The dimensions of MN1 were set to W_{MN1}=1 μm and L_{MN1}=5 μm, allowing to determine the output voltage of the amplifier I_1.

$$v_{GS,MN1} = \sqrt{\frac{2i_C L}{k_n W}} + V_{T,n} = \sqrt{\frac{(2)(26.316\mu)(5\mu)}{(100\mu)(1\mu)}} + 0.55 \simeq 2.17V$$

$$v_{G,MN1} = v_{GS,MN1} + v_{S,MN1} = 2.17 + 0.1 = 2.27V$$

$$g_1 = \frac{v_{G,MN1}}{V_i - V_{ref}} = \frac{2.27}{1.2 - 0.1} \simeq 2.1$$

A similar process was used to design the remaining MOSFETs, having in mind that since

the circuit is essentially a current mirror, MP0 and MP1 have the same dimensions. The only difference was that the amplifier I_2 gain was set to 1 and the dimensions of MP2 were calculated.

MN0 is essentially a switch that has to be able to lower the gate of MN1 to approximately 0 V when the CLK signal goes high in order to cut-off the current flow during the capacitor discharge. So it was set with W_{MN0}=10 μm and L_{MN0}=5 μm, which proved to be enough to perform the desired operation. Due to the ideal characteristics of the amplifiers used, a dummy resistor R0 had to be added at the output of I1, in order to allow the gate of MN1 to reach 0 V when connected to the ground. When the amplifiers are replaced by more realistic models, that resistor will be no longer necessary. MN2 is also a switch, whose triode resistance value is important for the discharge process of the C_{S1} capacitor. Considering that $5\tau = 5$ ns and $C_{S1} = 2.5$ pF. Therefore

$$R_{MN2} = \frac{\tau}{C_{S1}} = \frac{1n}{2.5p} = 400\Omega$$

Using equation 5.2 yields

$$\left(\frac{W}{L}\right)_{MN2} = \frac{1}{k_n r_{on}(v_{GS} - V_{T,n})} = \frac{1}{(100\mu)(400)(3-0.55)} \simeq 10$$

For simplicity, setting $L_{MN2} = 1$ μm results in $W_{MN2} = 10$ μm.

The summary of all the results obtained are presented in table 5.6. A sample of the sawtooth wave generator output is shown in figure 5.8.

Table 5.6: Sawtooth generator main parameters

Component	Value	Units
MN0	W=10;L=5	μm
MN1	W=1;L=5	μm
MN2	W=10;L=1	μm
MP0	W=2.5;L=1	μm
MP1	W=2.5;L=1	μm
MP2	W=1.5;L=1	μm
CS1	2.5	pF
R1	3800	Ω
g1	2.1	-
g2	1	-

From 1.2 V the wave reaches a peak voltage of 1 V and for 0.9 V, of approximately 0.5 V. Essentially, the amplitude of the sawtooth wave is 1 ± 0.5 V for $V_i = 1.2 \pm 0.3$ V. The command signal ϕ_1 is generated with a variable duty-cycle which is defined according to the amplitude of the sawtooth wave, as expected.

5.2.4 Oscillator

In order to set the switching frequency to 10 MHz and generate the ϕ_2 signal and the sawtooth wave clock, a ring oscillator was designed. The functional model schematic is shown in figure 5.9.

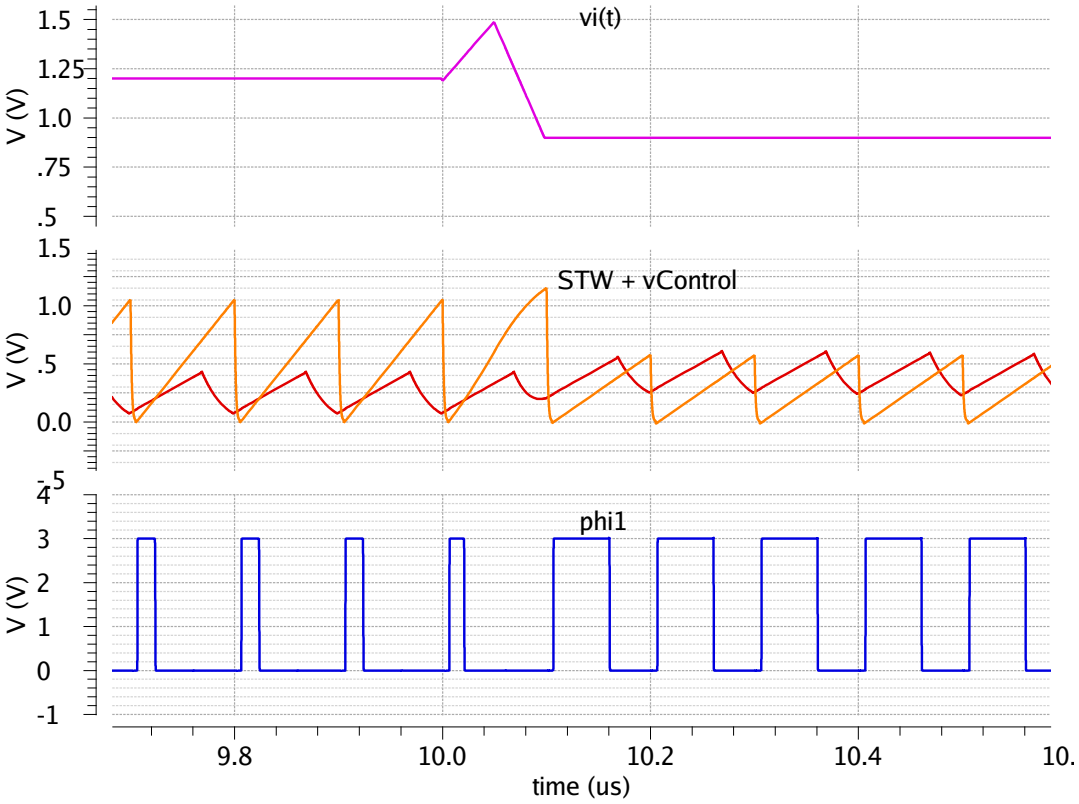

Figure 5.8: Sawtooth wave generator output sample.

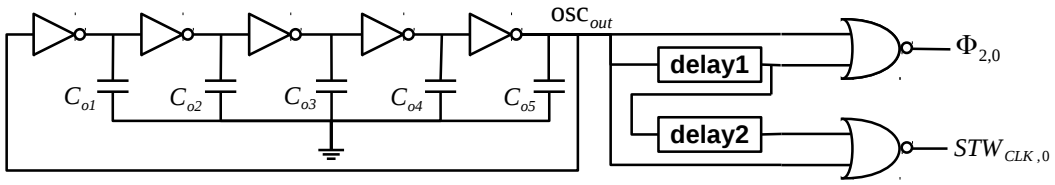

Figure 5.9: Oscillator functional model.

The oscillator was employed with a closed-loop chain of inverters which generates a signal with a frequency of 10 MHz and a 50 % duty-cycle. Then, is delayed once and both the original and NOR operation is performed with the original and delayed signal, producing $\phi_{2,0}$. The first delay is adjusted in order for $\phi_{2,0}$ to have a 30 % duty-cycle. Then, the signal is further delayed and a second NOR operation is performed to produce the signal $STW_{CLK,0}$. The second delay is adjusted in order for $STW_{CLK,0}$ to have a 5 % duty-cycle. The timing diagram is shown in figure 5.10.

The designed oscillator is shown in figure 5.11.The oscillating frequency is given by equation 5.8.

$$f_{osc} = \frac{1}{N(t_{pHL} + t_{pLH})} \tag{5.8}$$

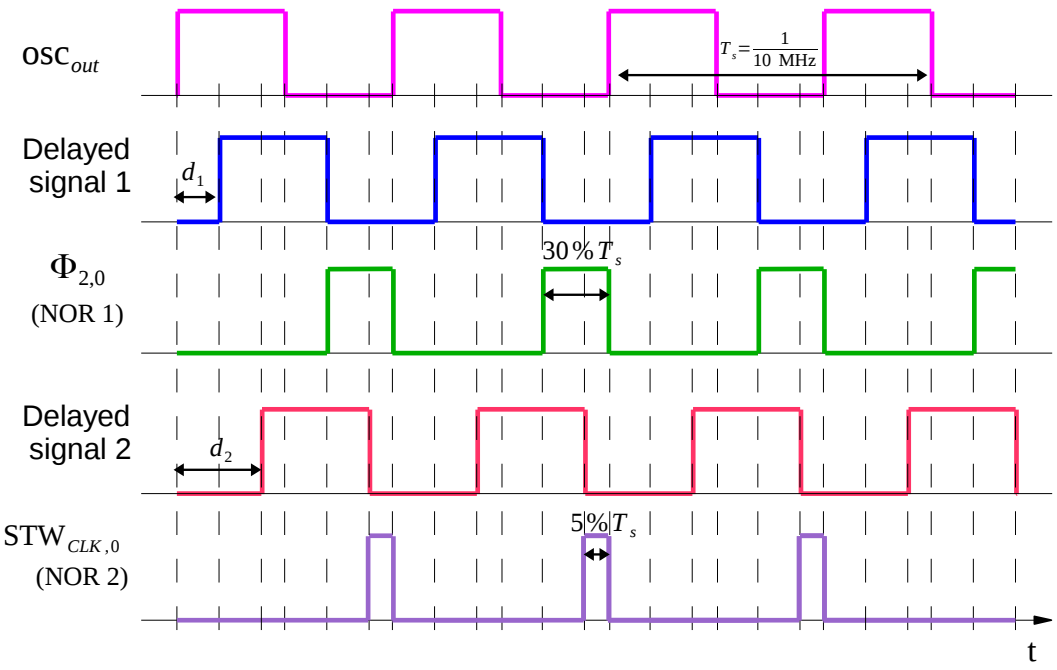

Figure 5.10: Oscillator timing diagram.

where N is the number of inverters in the chain, t_{pHL} is the propagation time from the logic level high to low and t_{pHL} is the propagation time from the logic level low to high between the input and the output of each inverter. In literature [3], it was stated that the ring oscillator works best for a minimum of five inverters. So N was set to 5. Since the desired duty-cycle of the base square wave is 50% and the period is $T_s = 1/10M = 100$ ns, then each MOSFET dimensions were adjusted, as well as the C_o capacitors value, in order to have $t_{pHL} = t_{pLH} = 50/5 = 10$ ns. A summary of the results is depicted in table 5.7.

Table 5.7: Oscillator parameters.

Component	**Value**	**Units**
PMOS	W=3.1; L=1	μm
NMOS	W=1.5; L=1	μm
C_{o1-5}	1	pF

To generate the signals $\phi_{2,0}$ and $STW_{CLK,0}$, the dimensions of the MOSFETS in the delay cells, as well as the value of the capacitors C_{d1} e C_{d2} was adjusted, until the desired duty cycle values were achieved. A summary of the delay cell parameters are shown in table 5.8.

The transistor parameters used in the NOR gates are depicted in table 5.9. They were chosen in order to minimize the time delays inserted by the logic gate while appropriately performing the NOR operation. These parameters were also used to design the remaining NOR gates used in the project.

A sample of the oscillator block final output is shown in figure 5.12, where signals $\phi_{2,0}$ and

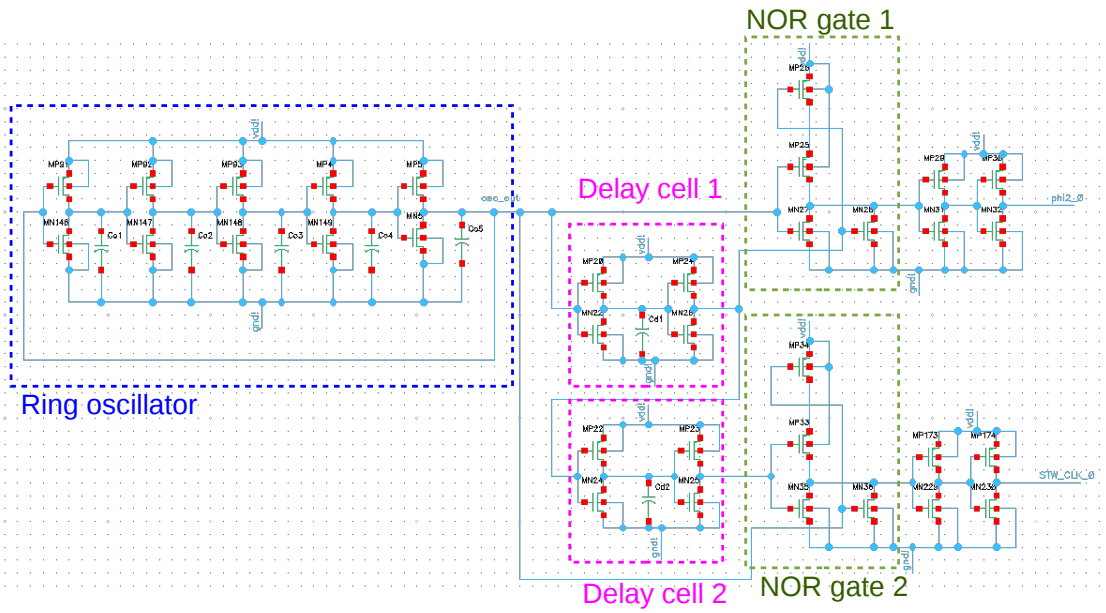

Figure 5.11: Main oscillator, $\phi_{2,0}$ and $STW_{CLK,0}$ generator schematic.

Table 5.8: Delay cells 1 and 2 parameters.

Component	Value	Units
MP20, MN22	W=1.5; L=1	μm
MP22, MN24	W=1; L=1	μm
MP23, MP24, MN25, MN26	W=10; L=1	μm
C_{d1}	1	pF
C_{d2}	1.3	pF

Table 5.9: NOR gate parameters.

Component	Value	Units
MP25, MN26	W=20; L=1	μm
MN27, MN28	W=5; L=1	μm

$STW_{CLK,0}$ are depicted, and it can be seen that the period, as well as the signal duty-cycles are approximately 100 ns, 30 % and 5 %, respectively.

5.2.5 Dead time generator

The dead time generator implemented is shown in figure 5.13. It operates with the same principle described in chapter 3 subsection 3.2.

$\phi_{2,0}$, which is delayed once, by the delay cell 3, resulting in the control signal ϕ_2. Further delay is applied, by the delay cell 4. Then, the delayed signal and $\phi_{2,0}$ are submitted to a logic OR operation resulting in $\phi 2_{control}$ which is on during the dead time and also when ϕ_2 is high.

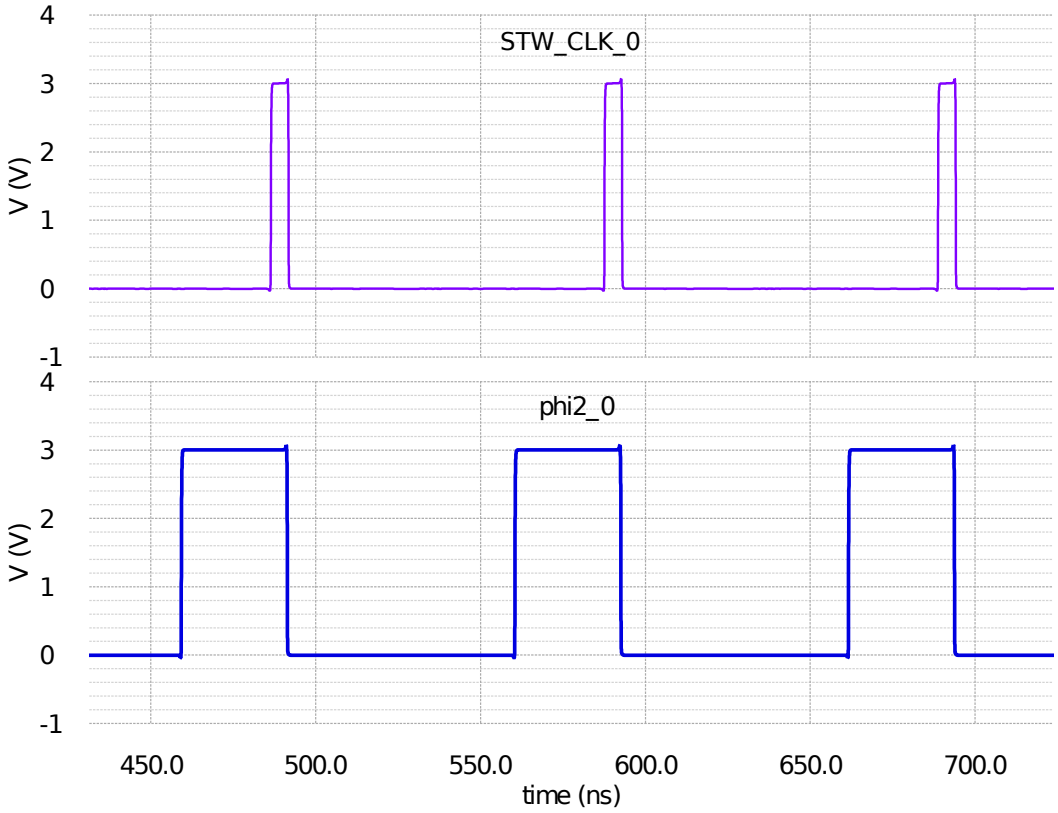

Figure 5.12: Oscillator output sample.

$\phi 2_{control}$ is then used to prevent ϕ_1 and ϕ_2 from being high at the same time through the following mechanism: if $\phi 2_{control}$ (ϕ_2+2×dead time) is high, the switches MN3 and MP3 open, blocking the transmission of $\phi_{1,0}$. Meanwhile, MN4 acts as a pull-down resistor, to ensure that ϕ_1 goes to (or very close to) 0 V, during the time that MN3 and MP3 are open. If $\phi 2_{control}$ is low, $\phi_{1,0}$ signal is transmitted. Summarizing:

$$\phi_1 = \begin{cases} 0V & \text{if } \phi_{2,0} \text{ is high} \\ \phi_{1,0} & \text{if } \phi_{2,0} \text{ is low} \end{cases} \tag{5.9}$$

MP3, MN3 and MN4 were chosen with a size large enough that ensured the performance of the desired operations. No calculations were necessary. They were set with W=10 μm and L=1 μm.

To perform the OR operation, a NOR gate followed by a NOT gate was employed. The standard NOT gate dimensions used in the project are the ones listed in table 5.10. Once again these dimensions were chosen for practical purposes, since the resultant time delays were neglectable and the NOT operation was performed appropriately.

The delay cell 3 parameters are shown in table 5.11. The delay cells 3 and 4 have equal parameters, since they generate the same time delay.

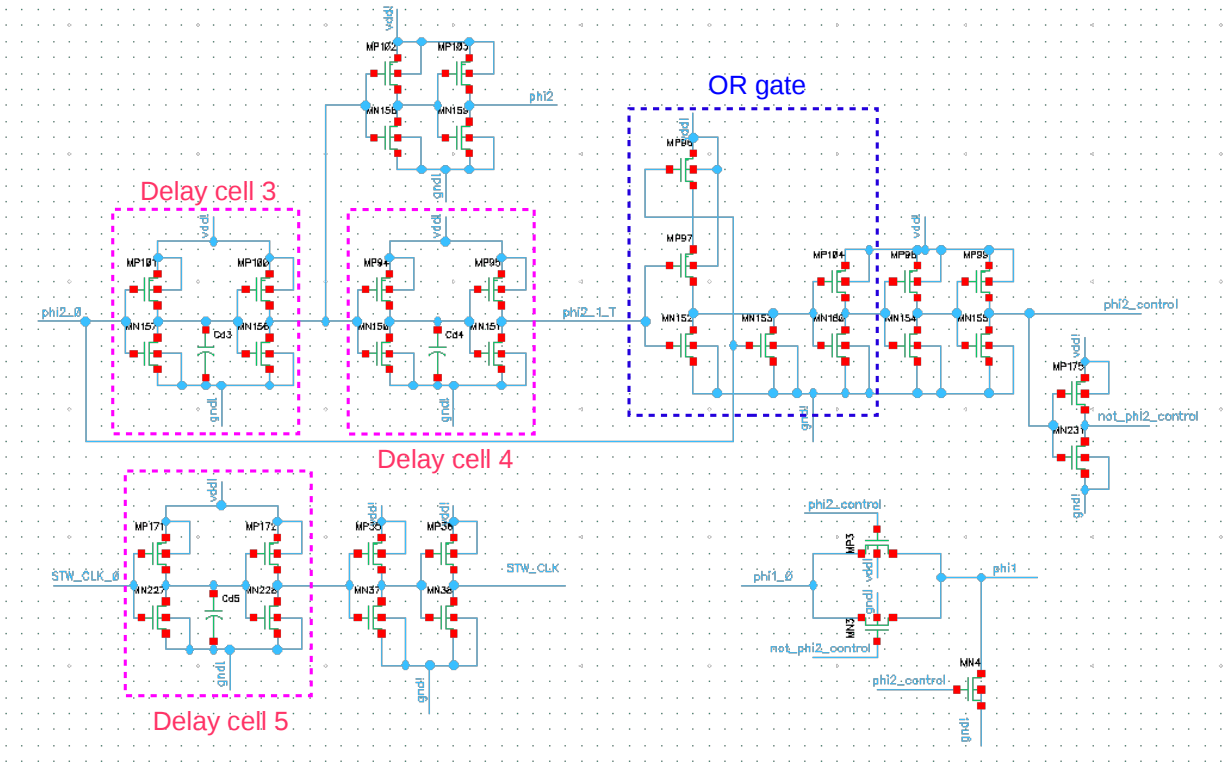

Figure 5.13: Dead time generator schematic.

Table 5.10: Standard NOT gate parameters.

Component	W	L	Units
PMOS	10	1	μm
NMOS	5	1	μm

Table 5.11: Delay cell 3 parameters.

Component	Value	Units
MP101	W=3; L=1	μm
MP100	W=10; L=1	μm
MN157	W=1.5; L=1	μm
MN156	W=5; L=1	μm
C_{d3}	1	pF

The signal $STW_{CLK,0}$ is also delayed, by delay cell 4, producing STW_{CLK}, in order to synchronize ϕ_1 (which is indirectly generated through STW_{CLK}) and ϕ_2.

5.2.6 Converter MOSFET drivers

Since the MOSFETs present in the converter have large dimensions, they also have large parasitic capacitances. In order to achieve fast switching speeds, these capacitances have to be charged with

sufficient amount of current. The closed-loop control generates the necessary voltage signals, but does not supply the necessary amount of current to charge the parasitic capacitances. Therefore, a driver that increases the current drive capability of the regulation block is needed. The basic MOSFET driver used in this project is shown in figure 5.14.

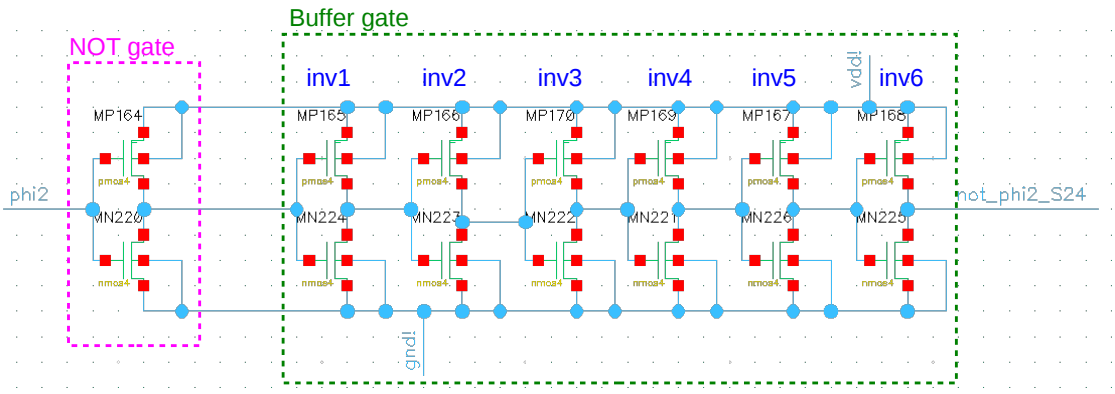

Figure 5.14: Basic MOSFET driver.

It consists of a NOT gate, when it is necessary to invert the input signal, and a buffer gate to amplify the current. The buffer gate was designed with a chain of inverters of increasing size as the chain progresses. Therefore, being i the current inverter, the next inverter dimensions are given by

$$\left(\frac{W}{L}\right)_{i+1} = K\left(\frac{W}{L}\right)_{i} \tag{5.10}$$

The practical rule K = $e \simeq 2.72$ was used, since the total minimum propagation time of the inverter chain occurs for this K value [25]. The dimensions of the buffer gate employed in the driver are listed in table 5.12.

Table 5.12: MOSFET driver buffer parameters.

Inverter n^o	**PMOS dimensions (μm)**	**NMOS dimensions (μm)**
1	W=10; L=1	W=5; L=1
2	W=27.2; L=1	W=13.6; L=1
3	W=74; L=1	W=40; L=1
4	W=201; L=1	W=109; L=1
5	W=550; L=1	W=296; L=1
6	W=1450; L=1	W=805; L=1

A driver was designed for each transistor set, making up a total of ten drivers. Not all the buffer gates were designed with six inverters, since not all the MOSFETs have the same size or switch sets have the same amount of transistors, which means that not all the drivers need to have the same current drive capability. Sets with less or smaller MOSFETs required buffer gates with four inverters, the remaining ones required six.

5.2.7 System overview

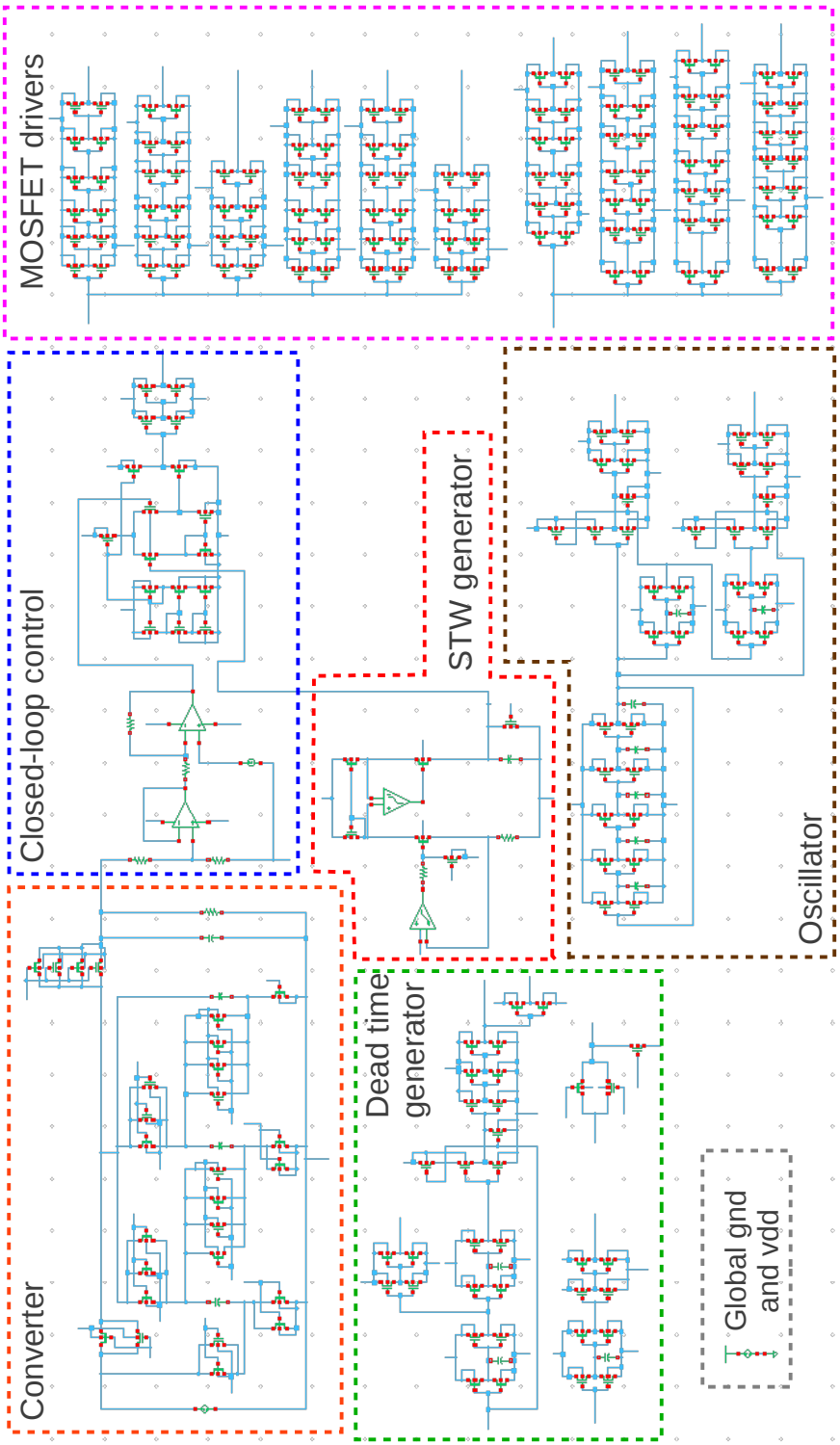

Figure 5.15: System overview.

5.3 Simulation results

After the system design, a series of tests were performed. In this section there are shown the main tests made and the primary results obtained.

5.3.1 Nominal conditions

The main goal of the converter is to guarantee a 2.5 DC voltage at the output when the input is 1.2 V supplying a 100 mA current. The first test was made in these conditions. The load resistor $R_L = 25\ \Omega$ ensures that if the output is 2.5 V, the load current will be 100 mA. The output voltage is shown in figure 5.16.

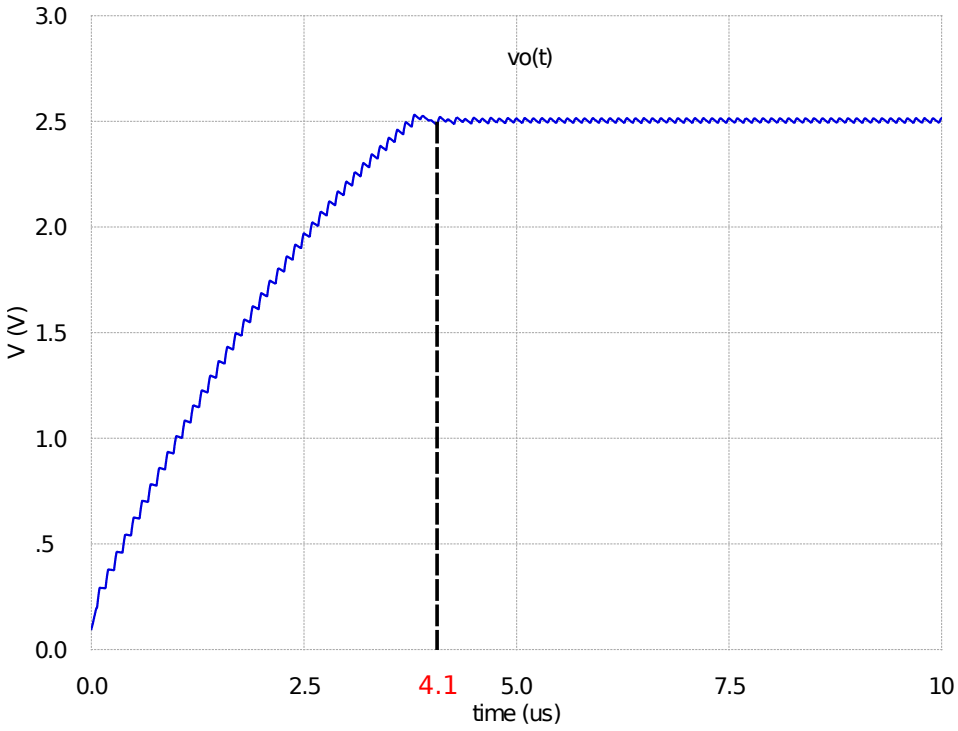

Figure 5.16: Converter response during nominal operation conditions ($V_i = 1.2$ V and $I_o = 100$ mA).

The steady state begins at approximately 4.1 μs, but beyond 5 μs the voltage ripple stabilizes and the output voltage is maintained ate 2.5 V as desired. The ripple will be further analysed in the following tests.

5.3.2 Variable input voltage

To test the line regulation of the converter, the input voltage was stepped from 1.2 V to 0.9 V and then to 1.5 V and then again to 1.2 V. The converter response was tested for the minimum, nominal and maximum input voltage because if the converter response is satisfactory for the nominal and bound input voltages it is also expected to work for other values as well. The response of the

converter is shown in figure 5.17. A closer view of the response in order to analyse the voltage ripple is shown in figure 5.18.

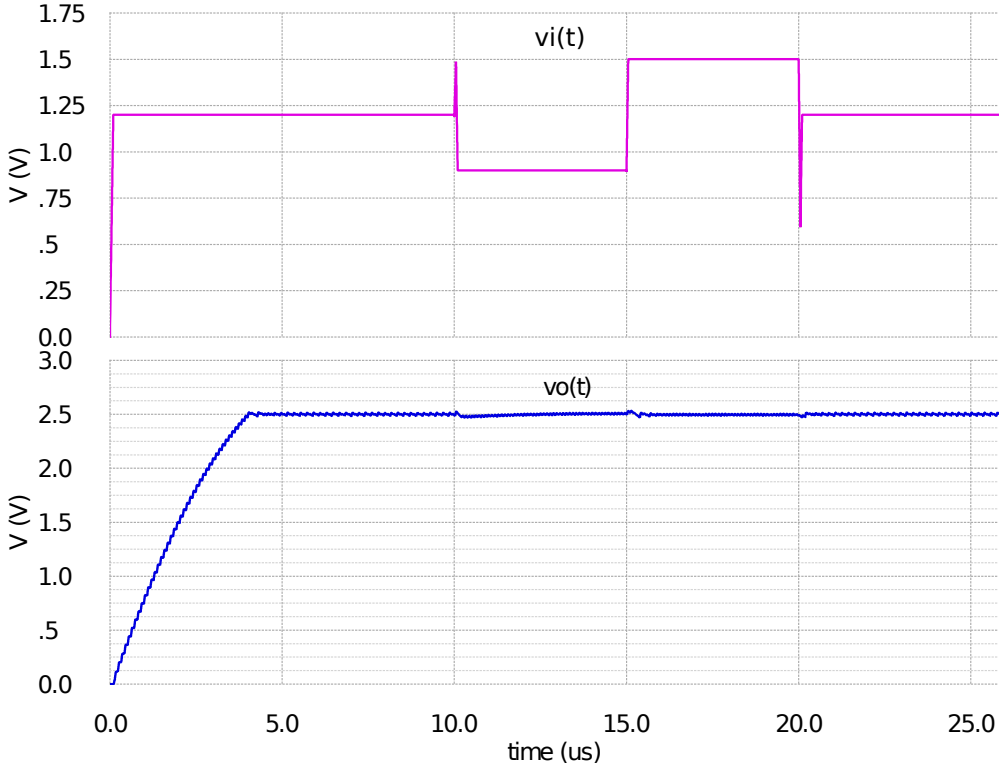

Figure 5.17: Converter response during line variations.

Analysing 5.17 it seems that despite of the line variations, the DC value is maintained around 2.5 V and the voltage ripple also remains constant. However, having a more closer look to the output voltage wave, as is depicted in figure 5.18, it is visible that the DC value has a slight positive deviation for $V_i = 0.9$ V and a negative deviation for $V_i = 1.2$ V and for $V_i = 1.5$ V. The ripple remains approximately the same for the minimum and maximum input voltage, but has a larger value for the nominal voltage. A more detailed analysis is depicted in table 5.13, where the ripple and DC values for each input voltage are presented. Overall, the converter response to line variations is good. In most applications this slight deviations from 2.5 V are acceptable and the ripple is smaller than 1 % in all cases.

Table 5.13: Output voltage ripple analysis for different values of V_i.

v_i(t) (V)	DC value (V)	Deviation from 2.5 V (%)	ΔV_o(%)
0.9	2.504	+0.16	0.43
1.2	2.499	-0.04	0.72
1.5	2.494	-0.24	0.42

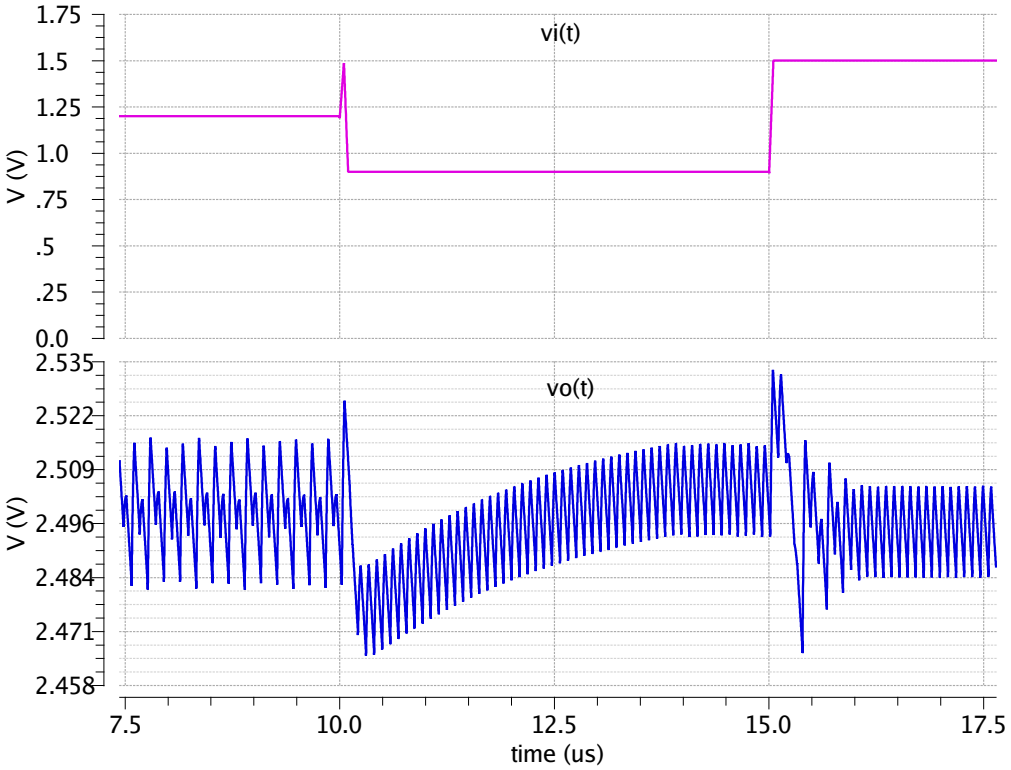

Figure 5.18: Converter response during line variations: ripple analysis.

5.3.3 Variable load

To test the load regulation of the converter, the load current was stepped from 100 mA to 10 mA, to 150 mA, then to 50 mA and finally to 0 mA. This way the response of the converter is tested for the nominal load, 10 %, 50 % and 150 % (overload) and no load situations. The results are shown in figure 5.19. A closer view of the response in order to analyse the voltage ripple is shown in figure 5.20.

Analysing 5.19, despite some overshoots during load steps, the output DC voltage is maintained near to 2.5 V. But the ripple changes with the load current. Having a closer look to the output voltage wave, as is depicted in figure 5.20, it can be seen that the DC value has small deviations from 2.5 V which go from -0.44 % for $I_o = 150$ mA to +1.04 % for 0 mA. From this figure it is also visible that the voltage ripple is very small for small loads and increases for higher loads. For load currents equal or smaller than 100 mA, the voltage ripple is <1 %. But for an overload situation, the ripple may be greater than 1 %, since for $I_o = 150$ mA it has an approximate value of 1.16 % The results of the ripple and output DC voltage analysis are depicted in table 5.14.

5.3.4 Energy efficiency

In order to determine the converter's energy efficiency, the input (P_i) and output (P_o) power consumptions were computed based on simulation results. The system was tested for line and load

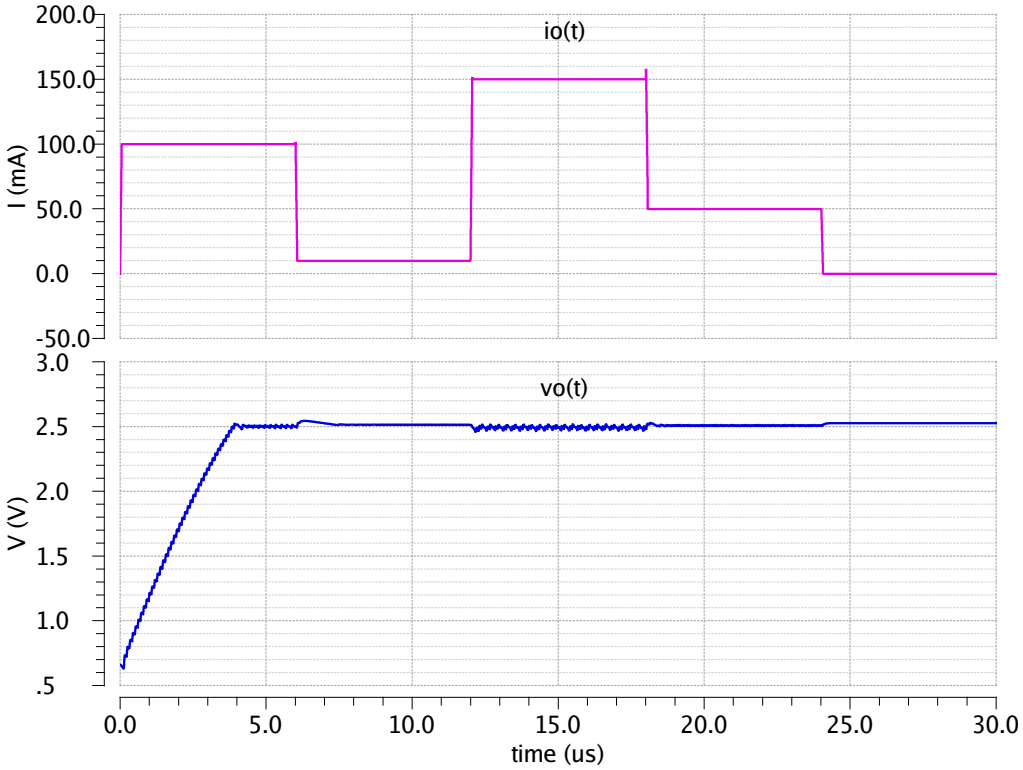

Figure 5.19: Converter response during load variations.

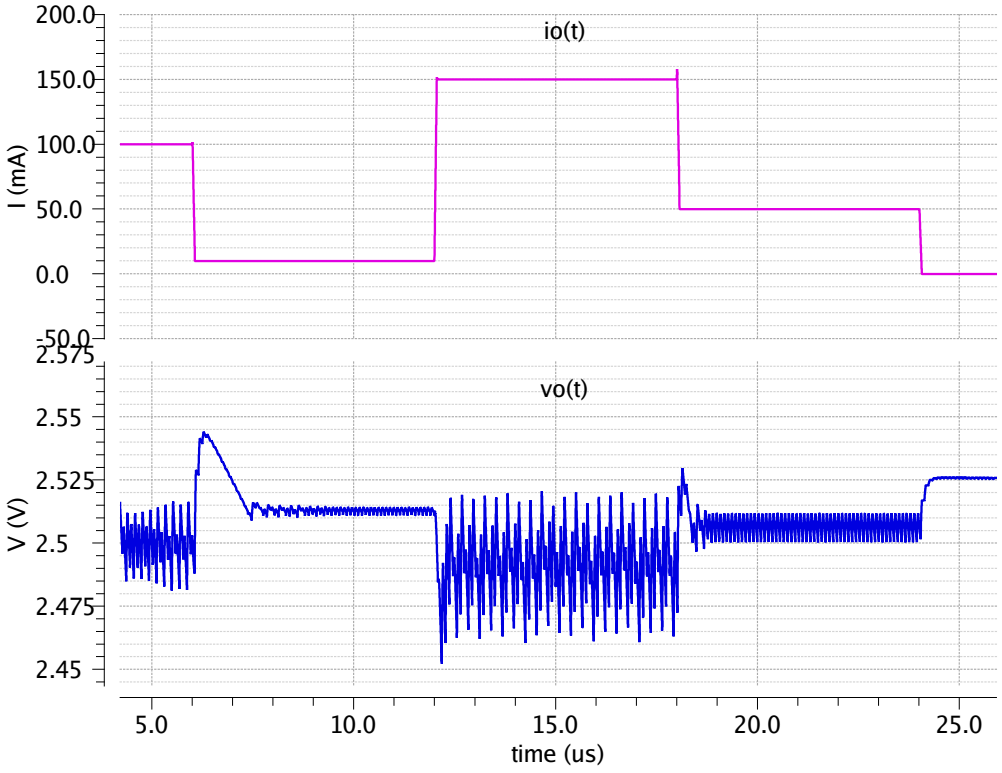

Figure 5.20: Converter response during line variations: ripple analysis.

Table 5.14: Output voltage ripple and DC value analysis for different values of I_o.

I_o (mA)	DC value (V)	Deviation from 2.5 V (%)	$\Delta V_o(\%)$
0	2.526	+ 1.04	0.01
10	2.513	+ 0.52	0.08
50	2.506	+ 0.24	0.23
100	2.499	- 0.04	0.70
150	2.489	- 0.44	1.16

variations and the energy efficiency was determined using equation 5.11.

$$\eta(\%) = \frac{P_o}{P_i} \times 100\% \tag{5.11}$$

For variable load, the input/output current ratio remained the same, so the converter efficiency does not change considerably with variable loads. However, input voltage variations affect the energy efficiency. From simulation results, plotted in figure 5.21, it can be seen that the maximum efficiency occurs for $V_i = 0.9$ V. It has the lowest value around the nominal input voltage and then increases until $V_i = 1.5$ V is reached.

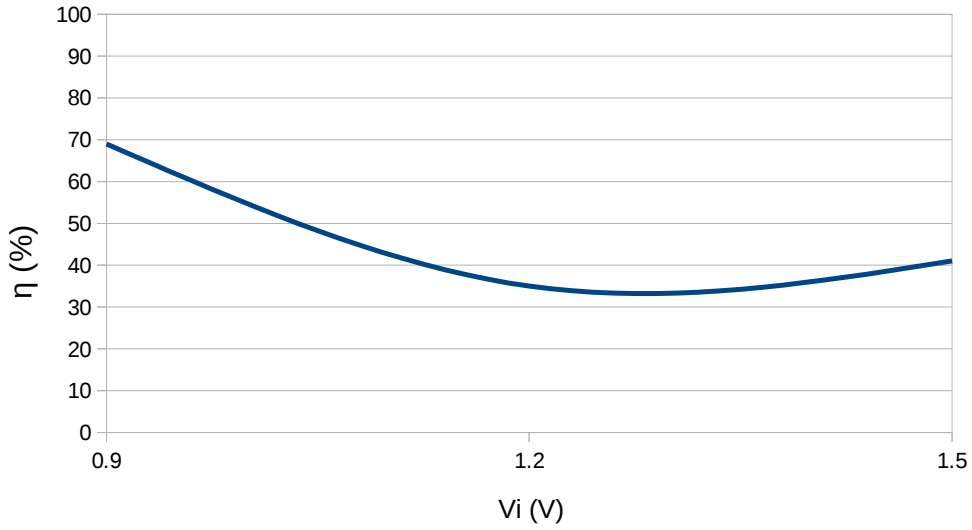

Figure 5.21: Energy efficiency vs input voltage.

For the nominal input voltage, the converter's energy efficiency is below 40 %. Some switched-capacitor converters can achieve an energy efficiency above 90 % [26], but mainly when regulated with an open-loop control. With a closed-loop control, specially when the converter has line and load regulation capabilities, a lower efficiency is a frequent consequence [13].

5.3.5 Power supply rejection ratio (PSRR)

The power supply rejection ratio (PSRR) is an important parameter in voltage regulators. It defines the amount of noise that the device can reject from the power supply, and is given by

$$PSRR(db) = 20log\frac{\Delta V_{o,pk-pk}}{\Delta V_{i,pk-pk}} \tag{5.12}$$

To perform the tests, it was assumed that the input voltage had 20 % noise, which corresponds to $V_{i,pk-pk} = 0.24$ V, and the noise frequency was varied from 1 Hz to 10 GHz. The simulation results are depicted in table 5.15 and the corresponding graphical plot is shown in figure 5.22.

Table 5.15: PSRR for $V_i = 1.2$ V with 20 % of noise.

Noise frequency (Hz)	max	min	PSRR (db)
10^0	2.516	2.481	-16.60
10^1	2.517	2.482	-16.84
10^2	2.516	2.481	-16.71
10^3	2.516	2.481	-16.85
10^4	2.516	2.480	-16.52
10^5	2.510	2.486	-19.79
10^6	2.521	2.480	-15.52
10^7	2.513	2.481	-17.31
10^8	2.517	2.481	-16.42
10^9	2.517	2.480	-16.38
10^{10}	2.513	2.480	-17.30

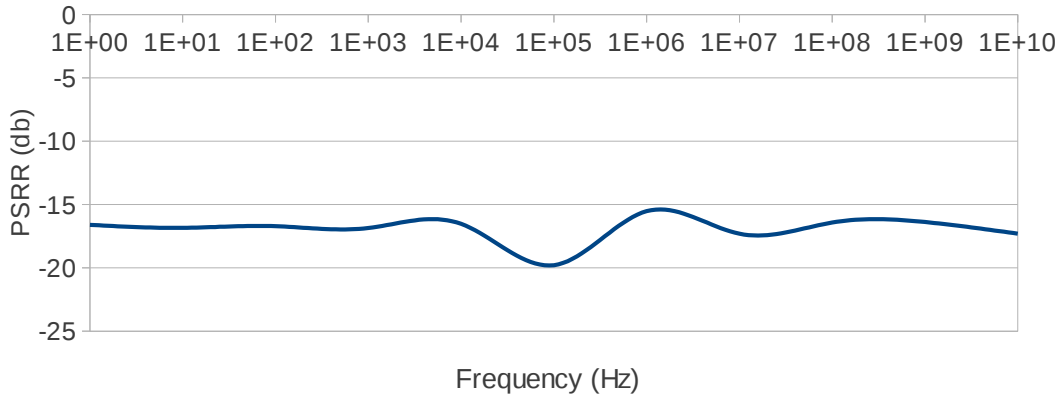

Figure 5.22: PSRR vs input voltage noise frequency.

More negative PSRR values represent a higher rejection ratio. Thus, the converter has a higher PSRR when the input voltage has a noise frequency around 100 kHz, corresponding to a value of approximately -20 dB. Also, it has a lower PSRR for 1 MHz, corresponding to -15.5 dB. However, despite of this oscillations, the overall rejection ratio rounds -17 dB.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

Overall, the converter and the regulation block showed a good performance even in the presence of line and load variations. The output response for line variations was slightly better, since with no load current the output DC voltage deviated around 1.04 % from 2.5 V. These small deviations in the DC value are acceptable for most applications, unless a high precision voltage regulation is required. In all tests performed, the output voltage ripple was below 1 % or very close to that value. All functional specifications of the converter were met, the output was regulated to 2.5 V for an input voltage of 1.2 ± 0.3 V and a current drive capability of 100 mA was achieved. To ensure the radiation hardening features, a lot of ideas were conceived, which will be presented in the next section, but only a few were implemented. Mainly, PMOS transistors were employed whenever possible and the converter size reduction was a concern, since smaller devices are less likely to be hit by high ionizing particles. The employment of digital electronics was reduced to a minimum and was decided to use an external reference source, since, as stated in chapter 2, internal voltage sources are more susceptible to deviations when submitted to ionizing radiation.

A great amount of time was spent deducing the converter model and designing the converter switches. There is a variety of step-up charge-pump topologies described in papers, but few mathematical analysis are found and the ones existent often do not consider the load capacitor or load resistor in the model, in order to simplify the analysis. But the inclusion of these elements in the model is important. Charge-pump based converters exist for many years now, but most of them were designed with open-loop control, which limited the output voltage step capabilities and made the converter response susceptible to line variations. It is not new technology, but began to receive more attention in recent years. Unlike inductor converters, where the basic operation theory is well covered in literature, the main source of information for step-up switched-capacitor converters is found in papers and academic dissertations, which has the advantage of providing state of the art information, but also has disadvantages. Some concepts are not very clearly explained and even some of them are not quite well established, specially around the closed-loop output regulation subject.

Some time was spent trying to obtain higher on-resistance values for the converter MOSFETs since small on-resistance leads to larger dimensions and a higher number of parallel connected MOSFETs, with larger parasitic capacitances and drive currents.

Meanwhile, the behavioural simulations in Simulink were performed . The regulation took some time to study and a great amount of research was necessary. A number of simulations were performed with the classic sawtooth-based control but, the converter response was not resilient to line variations. Then, other solutions, such as a current-based control, were tried with similar overall results. Finally, the control based on the variable sawtooth wave was tried, with good results.

After the system parameters design, topology and regulation block validation through behavioural simulations, the simulations in Cadence began. Some difficulties were found when replacing the ideal switches with transistors, mainly because in this type of converters the gate-source voltages are constantly floating and the MOSFET design, as well as guaranteeing the proper switching, becomes a little more challenging.

Due to a time shortage, it was not possible to continue the design and replacement process of all the functional components, which precluded the performance of the system layout and implementation of the main radiation hardening features.

During the performed research, it was difficult to encounter mathematical models that could be used in this project, since usually each author performs the analysis for a specific application. When that section of the current project was developed, that factor was kept in mind. Therefore, the mathematical model, system parameter extraction and converter MOSFETs design algorithms can be adapted and reused to design a new converter with different system requirements.

6.2 Future work

The first step would be to solve the issues in the amplifier model developed and replace all the functional operational amplifiers. For the radiation hardening there are several things to be done. The first one would be to replicate the digital section of the system and develop a voting mechanism, in other words, apply a redundancy technique to the section of the control responsible for generating the command signals ϕ_1 and ϕ_2.

In the triode region, for the same equivalent on-resistance, the NMOS transistors have smaller dimensions then PMOS, which at first glance makes them the right choice to design a compact converter. However, NMOS are more susceptible to ionizing radiation effects than PMOS transistors, which can be mitigated by employing special layout techniques. But, the occupied area is larger compared with a NMOS design with conventional layout techniques. So, concerning the final chip area vs radiation hardening features, the choice between PMOS and NMOS transistors is not very obvious. The PMOS transistors employed in the converter were in a considerable large number and had high dimensions, mainly because they were designed to function in the worst cases. In other words, since the converter nodes have significant voltage swings, specially when the input voltage changes, it is difficult to establish a constant gate-source voltage value. Thus, the

MOSFETs were designed to operate with both low and high gate-source voltage values. But, to ensure this wide operation range, the resulting MOSFET dimensions were a little high. A possible solution is to replace all the switches, except the ones directly connected to the ground terminal, by the switch cell presented in chapter 2, subsection 2.2.2.1. This way, most of the switches would be implemented with PMOS transistors, whose operation is more robust to ionizing radiation, but would have smaller dimensions than the current PMOS switches, since this switching mechanism guarantees a gate-source voltage very near to vdd and independent of the node voltage swings. Therefore, the PMOS can be designed with smaller dimensions and in less number. In the commutation circuit a NMOS is always present, but the size of this transistor is much smaller than the NMOS employed as a switch in the converter. So, one of the first things to do would be to analyse if this solution is more viable than the one employed in the project. For the external capacitors, based on the information presented in 2, subsection 2.4.3, a good solution would be to employ glass capacitors.

Finally, perform the layout of all the components, using special layout techniques to ensure the radiation hardening features, such as the annular layout presented in chapter 2 subsection 2.4.2, or other state of the art solutions. Employ guard rings to prevent latch-up effects. It would also be interesting to improve the produced source code, specially the parameter extraction program, with optimization algorithms, such as simulated annealing.

Appendix A

CMOS 0.35 μm process parameters extraction - raw data, calculations and plotting

In this appendix are shown the results of the DC analysis and the follow-up calculations made to determine the necessary process parameters, k_n, $V_{t,n}$, k_p and $V_{t,p}$, of 0.35 μm CMOS technology.

In the following analysis, when a given variable x_{ij} is presented, the index i represents the row number and j represents the column number of the table from which the original variable value was taken. $i, j \in \mathbb{N}$, but when one of the indexes is omitted, they are considered 0.

A.1 Simulation Results

Table A.1: V_{GS} values in function of I_D and W (larger values) for the NMOS transistor (V).

W (μm) \ I_D (mA)	0	0.1	0.5	1.0	1.5	2.0
1000	0	1.3183	3.0966	4.9493	6.5986	7.9207
2000	0	1.0915	2.1184	3.0965	4.0321	4.9492
3000	0	1.0159	1.7582	2.4553	3.0962	3.7216
4000	0	0.9471	1.5611	2.1186	2.6183	3.0963
5000	0	0.9033	1.4333	1.9063	2.3226	2.7151
6000	0	0.8681	1.3425	1.7579	2.1186	2.4552
7000	0	0.8426	1.2743	1.6473	1.9682	2.2649
8000	0	0.8223	1.2199	1.5608	1.8514	2.1187
9000	0	0.8056	1.1761	1.4910	1.7579	2.0021
10000	0	0.7930	1.1392	1.4332	1.6809	1.9063

Table A.2: V_{GS} values in function of I_D and W (larger values) for the PMOS transistor (V).

I_D (mA) / W (μm)	0	0.1	0.5	1.0	1.5	2.0
1000	0	-2.2404	-5.5501	-10.5982	-18.0661	-32.5328
2000	0	-1.7167	-3.5196	-5.5498	-7.8307	-10.5976
3000	0	-1.5048	-2.8347	-4.1863	-5.6059	-7.0271
4000	0	-1.3837	-2.4715	-3.5196	-4.5614	-3.5496
5000	0	-1.3203	-2.2403	-3.1131	-3.9201	-4.7231
6000	0	-1.2449	-2.0775	-2.8347	-3.5463	-4.1867
7000	0	-1.2003	-1.9550	-2.6298	-3.2533	-3.8058
8000	0	-1.1647	-1.8592	-2.4714	-3.0301	-3.5923
9000	0	-1.1355	-1.7812	-2.3448	-2.8534	-3.2949
10000	0	-1.1110	-1.7166	-2.2403	-2.6920	-3.1130

Table A.3: V_{GS} values in function of I_D and W (smaller values) for the NMOS transistor (V).

I_D (mA) / W (μm)	0	0.05	0.1	0.5	1.0	1.5
5	0	0.7934	0.9045	1.4450	1.9310	2.3589
10	0	0.7181	0.7937	1.1435	1.4417	1.6923
20	0	0.6627	0.7173	0.9506	1.1421	1.2986
50	0	0.6073	0.6470	0.7930	0.9041	0.9928
100	0	0.5729	0.6068	0.7170	0.7933	0.8525
200	0	0.5421	0.5725	0.6620	0.7173	0.7584
500	0	0.5045	0.5323	0.6069	0.6473	0.6752

Table A.4: V_{GS} values in function of I_D and W (smaller values) for the PMOS transistor (V).

I_D (mA) / W (μm)	0	0.05	0.1	0.5	1.0	1.5
5	0	-1.1165	-1.3130	-2.2577	-3.1486	-3.9706
10	0	-0.9853	-1.1179	-1.7280	-2.2552	-2.7112
20	0	-0.8937	-0.9843	-1.3888	-1.7229	-2.0000
50	0	-0.8109	-0.8704	-1.1127	-1.3052	-1.4605
100	0	-0.7648	-0.8116	-0.9824	-1.1119	-1.2152
200	0	-0.7263	-0.7657	-0.8930	-0.9820	-1.0517
500	0	-0.6821	-0.7161	-0.8119	-0.8701	-0.9134

A.2 β_n and β_p

In chapter 2, subsection 2.2.2, it was seen that

$$I_D = \frac{1}{2}\beta(|V_{GS}| - |V_T|)^2$$
$$\Leftrightarrow \sqrt{2I_D} = \sqrt{\beta}(|V_{GS}| - |V_T|)$$

β can be determined only by knowing the gate-source voltage and the drain current by making the following correlation:

$$\sqrt{2I_{D,i}} - \sqrt{2I_{D,i+1}} = \sqrt{\beta_{ij}}(|V_{GS,ij}| - |V_{GS,i(j+1)}|)$$

which yields

$$\beta_{ij} = 2 \times \frac{\sqrt{I_{D,i}} - \sqrt{I_{D,i+1}}}{|V_{GS,ij}| - |V_{GS,i(j+1)}|} \tag{A.1}$$

Table A.5: β_n values in function of I_D and W (larger values) (μA/V^2).

I_D (A) / W (μm)	0	0.1	0.5	1.0	1.5	2.0
1000	0	0.0966	0.0500	0.0371	0.0411	-
2000	0	0.2898	0.1793	0.1154	0.0854	-
3000	0	0.5546	0.3531	0.2459	0.1836	-
4000	0	0.8105	0.5520	0.4046	0.3142	-
5000	0	0.0887	0.7669	0.5830	0.4659	-
6000	0	1.3578	0.9943	0.7765	0.6337	-
7000	0	1.6396	1.2332	0.9810	0.8156	-
8000	0	1.9330	1.4764	1.1962	1.0049	-
9000	0	2.2261	1.7302	1.4181	1.2040	-
10000	0	2.5466	1.9715	1.6623	1.4136	-

Table A.6: β_p values in function of I_D and W (larger values) ($\mu A/V^2$).

I_D (A) / W (μm)	0	0.1	0.5	1.0	1.5	2.0
1000	0	0.0279	0.0067	0.0081	0.0003	-
2000	0	0.0940	0.0416	0.0194	0.0094	-
3000	0	0.1728	0.0939	0.0501	0.0355	-
4000	0	0.2582	0.1562	0.0931	0.0701	-
5000	0	0.3610	0.2253	0.1551	0.1113	-
6000	0	0.4408	0.2992	0.1995	0.1751	-
7000	0	0.5365	0.3768	0.2599	0.2352	-
8000	0	0.6335	0.4578	0.3236	0.2272	-
9000	0	0.7329	0.5401	0.3902	0.3683	-
10000	0	0.8332	0.6256	0.4951	0.4050	-

Table A.7: β_n values in function of I_D and W (smaller values) ($\mu A/V^2$).

I_D (mA) / W (μm)	0	0.05	0.1	0.5	1.0	1.5
5	0	0.0014	0.0010	0.0007	0.0006	-
10	0	0.0030	0.0025	0.0019	0.0016	-
20	0	0.0058	0.0056	0.0047	0.0041	-
50	0	0.0109	0.0143	0.0139	0.0128	-
100	0	0.0149	0.0252	0.0295	0.0287	-
200	0	0.0186	0.0382	0.0561	0.0598	-
500	0	0.0222	0.0549	0.1050	0.1298	-

Table A.8: β_p values in function of I_D and W (smaller values) ($\mu A/V^2$).

I_D (mA) / W (μm)	0	0.05	0.1	0.5	1.0	1.5
5	0	0.0004	0.0003	0.0002	0.0001	-
10	0	0.0010	0.0008	0.0006	0.0005	-
20	0	0.0021	0.0019	0.0015	0.0013	-
50	0	0.0048	0.0052	0.0046	0.0042	-
100	0	0.0078	0.0105	0.0102	0.0095	-
200	0	0.0111	0.0189	0.0217	0.0208	-
500	0	0.0148	0.0333	0.0506	0.0540	-

A.3 k_n and k_p

The intrinsic transconductance gain values for the NMOS and PMOS transistors are given by equations A.2 and A.3.

$$k_{n,ij} = \frac{\beta_{n,ij} L}{W_i} \tag{A.2}$$

$$k_{p,ij} = \frac{\beta_{p,ij} L}{W_i} \tag{A.3}$$

with $L = L_{min} = 0.35\ \mu$m.

Table A.9: k_n values in function of I_D and W (larger values) (μA/V^2).

W (μm) \ I_D (A)	0	0.1	0.5	1.0	1.5	2.0
1000	0	33.82	17.49	13.00	14.38	-
2000	0	50.71	31.38	20.20	14.94	-
3000	0	64.70	41.19	28.69	21.42	-
4000	0	70.92	48.30	35.40	27.50	-
5000	0	67.16	53.63	40.80	32.61	-
6000	0	79.20	58.00	45.29	36.97	-
7000	0	81.98	61.66	49.05	40.78	-
8000	0	84.57	64.59	52.34	43.96	-
9000	0	86.57	67.29	55.15	46.82	-
10000	0	81.21	69.48	57.62	49.48	-

Table A.10: k_p values in function of I_D and W (larger values) (μA/V^2).

W (μm) \ I_D (A)	0	0.1	0.5	1.0	1.5	2.0
1000	0	9.76	2.36	0.63	0.12	-
2000	0	16.45	0.28	3.40	1.64	-
3000	0	20.16	10.96	5.85	4.15	-
4000	0	22.60	13.67	8.14	6.14	-
5000	0	25.27	15.77	10.86	7.79	-
6000	0	25.71	17.46	11.64	10.21	-
7000	0	26.82	18.84	12.99	11.76	-
8000	0	27.72	20.03	14.16	9.94	-
9000	0	28.50	21.01	15.19	14.32	-
10000	0	29.16	21.90	17.33	14.18	-

Table A.11: k_n values in function of I_D and W (smaller values) ($\mu A/V^2$).

W (μm) \ I_D (mA)	0	0.05	0.1	0.5	1.0	1.5
5	0	97.37	73.22	50.85	38.62	-
10	0	104.99	87.44	67.51	56.30	-
20	0	100.75	98.24	81.87	72.22	-
50	0	76.17	100.35	97.34	89.89	-
100	0	52.25	88.07	103.28	100.59	-
200	0	32.49	66.79	98.15	104.68	-
500	0	15.56	38.41	73.52	90.88	-

Table A.12: k_p values in function of I_D and W (smaller values) ($\mu A/V^2$).

W (μm) \ I_D (mA)	0	0.05	0.1	0.5	1.0	1.5
5	0	31.11	23.97	15.13	10.46	-
10	0	34.17	28.73	21.60	17.00	-
20	0	36.60	32.68	26.91	23.02	-
50	0	33.90	36.44	32.40	29.34	-
100	0	27.43	36.68	35.78	33.14	-
200	0	19.36	32.99	37.93	36.36	-
500	0	10.37	23.32	35.44	37.83	-

A.4 $V_{T,n}$ and $V_{T,p}$

The threshold voltage of the MOSFETs can be given by equation A.4.

$$|V_{T,ij}| = |V_{GS,ij}| - \sqrt{\frac{2I_{D,j}}{\beta_{ij}}} \tag{A.4}$$

Considering that

$$V_{T,n} = |V_T|$$
$$V_{T,p} = -|V_T|$$

the threshold voltages of the NMOS and PMOS transistors for different drain current values and widths are given in tables A.13 and A.14.

Table A.13: $V_{T,n}$ values in function of I_D and W (larger values) (V).

I_D (A) / W (μm)	0	0.1	0.5	1.0	1.5	2.0
1000	0	-0.1203	-1.3763	-2.3893	-1.9475	-
2000	0	0.2607	-0.2431	-1.0663	-1.8959	-
3000	0	0.4154	0.0753	-0.3964	-0.9464	-
4000	0	0.4504	0.2152	-0.1048	-0.4715	-
5000	0	0.4749	0.2914	0.0542	-0.2150	-
6000	0	0.4843	0.3396	0.1530	-0.0572	-
7000	0	0.4933	0.3738	0.2195	0.0503	-
8000	0	0.5006	0.3969	0.2678	0.1235	-
9000	0	0.5059	0.4159	0.3034	0.1794	-
10000	0	0.5128	0.4272	0.3375	0.2242	-

Table A.14: $V_{T,p}$ values in function of I_D and W (larger values) (V).

I_D (A) / W (μm)	0	0.1	0.5	1.0	1.5	2.0
1000	0	0.4371	0.6372	22.6304	75.4979	-
2000	0	-0.2580	1.3817	4.5988	10.0549	-
3000	0	-0.4289	0.4284	2.1302	3.5809	-
4000	0	-0.5037	0.0588	1.1159	1.9790	-
5000	0	-0.5760	-0.1333	0.4779	1.2706	-
6000	0	-0.5713	-0.2495	0.3316	0.5933	-
7000	0	-0.5897	-0.3259	0.1445	0.3181	-
8000	0	-0.6028	-0.3812	0.0145	0.6040	-
9000	0	-0.6131	-0.4205	-0.0818	0.0005	-
10000	0	-0.6211	-0.4523	-0.2304	0.0295	-

Table A.15: $V_{T,n}$ values in function of I_D and W (smaller values) (V).

I_D (mA) / W (μm)	0	0.05	0.1	0.5	1.0	1.5
5	0	0.5253	0.4672	0.2717	0.0271	-
10	0	0.5355	0.5108	0.4234	0.3266	-
20	0	0.5309	0.5285	0.4883	0.4459	-
50	0	0.5114	0.5289	0.5248	0.5094	-
100	0	0.4911	0.5176	0.5329	0.5295	-
200	0	0.4687	0.5001	0.5284	0.5344	-
500	0	0.4374	0.4719	0.5093	0.5232	-

Table A.16: $V_{T,p}$ values in function of I_D and W (smaller values) (V).

I_D (mA) / W (µm)	0	0.05	0.1	0.5	1.0	1.5
5	0	-0.6421	-0.5487	-0.1069	0.5092	-
10	0	-0.6653	-0.6243	-0.4552	-0.2261	-
20	0	-0.6751	-0.6571	-0.5823	-0.4897	-
50	0	-0.6672	-0.6744	-0.6479	-0.6144	-
100	0	-0.6518	-0.6734	-0.6696	-0.6523	-
200	0	-0.6313	-0.6627	-0.6782	-0.6718	-
500	0	-0.5999	-0.6386	-0.6714	-0.6777	-

A.5 Process parameters curves for the converter's MOSFETs design

With the results from tables A.9, A.10, A.13 and A.14, the values of k_n, k_p, $V_{T,n}$ and $V_{T,p}$ were plotted, respectively. The results are shown in figures A.1 to A.4.

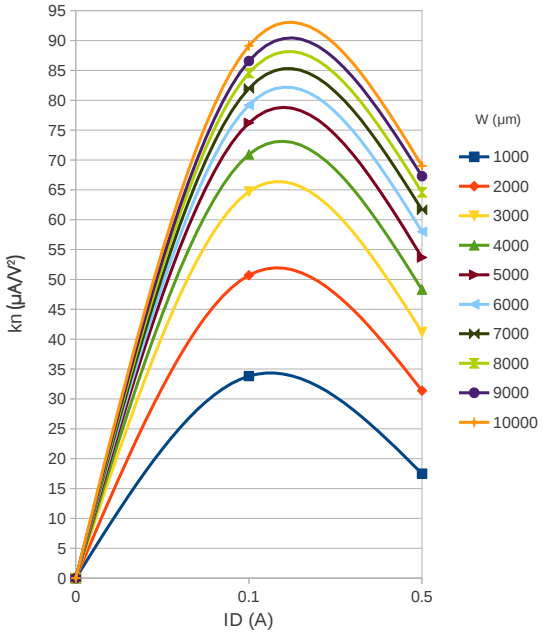

Figure A.1: CMOS 0.35 μm process parameters: k_n vs I_D.

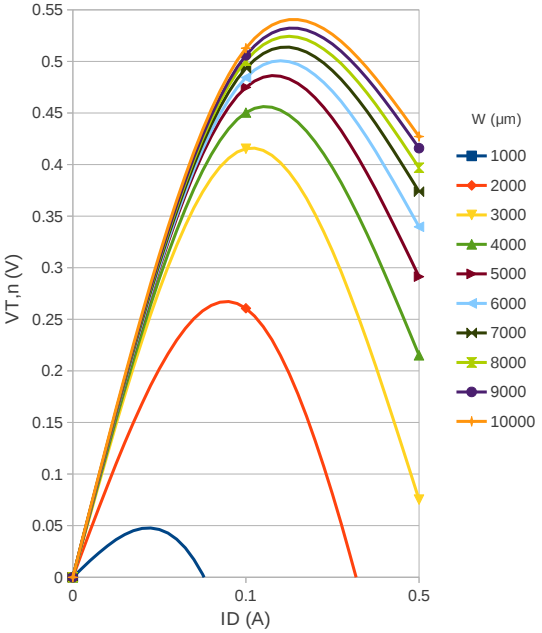

Figure A.2: CMOS 0.35 μm process parameters: $V_{T,n}$ vs I_D.

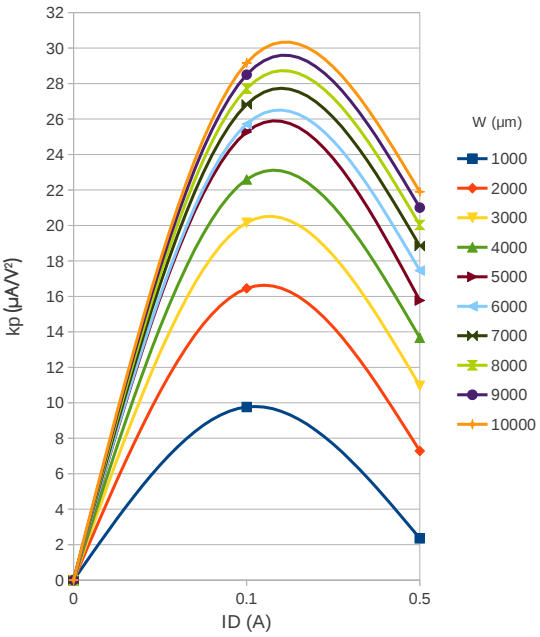

Figure A.3: CMOS 0.35 μm process parameters: k_p vs I_D.

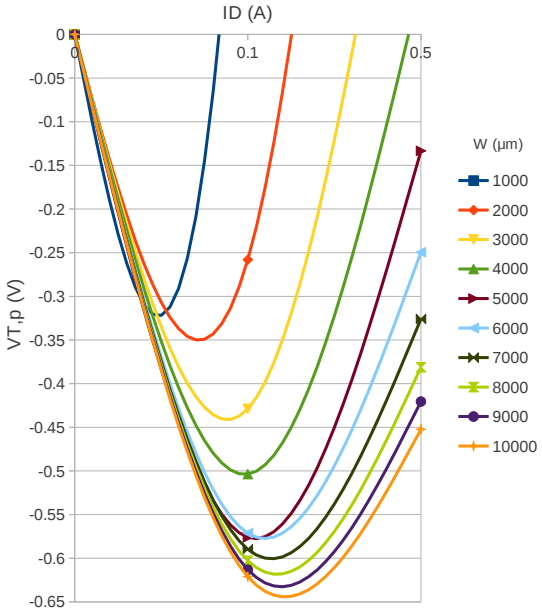

Figure A.4: CMOS 0.35 μm process parameters: $V_{T,n}$ vs I_D.

There are only shown the sections where the curves achieve the maximum or minimum value, according to the situation, since they represent the circumstances where a higher charge mobility is achieved and is convenient to design the MOSFETs to operate around that point.

Appendix B

Mathematical model of the system

In order to deduce the mathematical equations that approximately model the system, the circuit shown in figure B.1 was analysed. To simplify the analysis, the MOSFETs were modelled with switches.

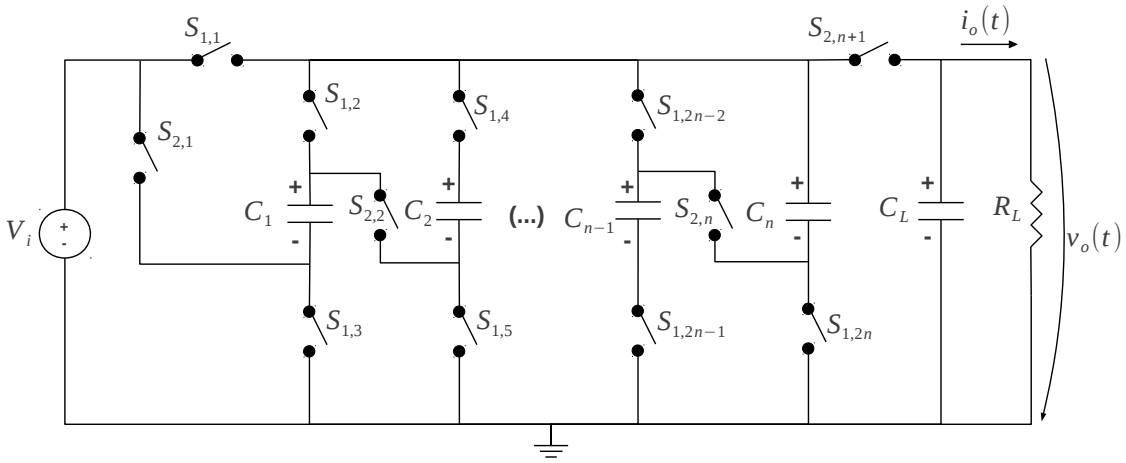

Figure B.1: Circuit used as a reference to deduce the mathematical model of the system.

When certain switches are on or off, the previous circuit can be represented by equivalent circuits, which will be analysed in detail in the following subsections. In this analysis, the switches are not considered entirely ideal, since when they are off, their internal resistance is considered infinite and when the switches are on, depending on the switch, their operation is modelled by resistors represented by r_{S1} and r_{S2}.

The operation of the converter during one working cycle can be divided into two stages. The first occurs when the switches $S_{1,i}|_{i\in[1,2n]}$ are on and takes place during the time interval $[t_0,t_1[$ which has a duration of $\Delta t_1 = DT_s$. The second stage occurs when the switches $S_{2,j}|_{j\in[1,n+1]}$ are on and takes place during the time interval $[t_1,t_2[$ where $\Delta t_2 = (1-D)T_s$. Each stage originates different circuits that can be analysed separately.

B.1 Operation during stage 1

When the $S_{1,i}$ switches are on, the circuit shown in figure B.1 becomes equivalent to the circuit in figure B.2.

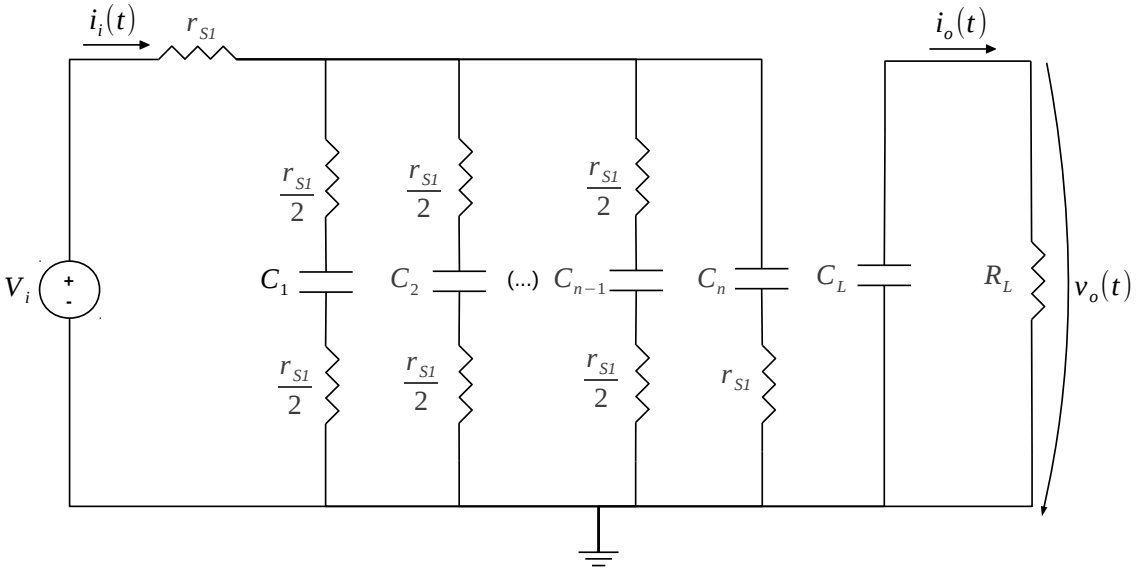

Figure B.2: Equivalent circuit during stage 1.

As it can be seen in the previous figure, in this first stage the load becomes cut-off from the input dividing the converter into two equivalent circuits. The first one represents the charging process of the flying capacitors and the second circuit represents the discharging process of the output capacitor. Each of these circuits will be analysed separately in the following subsections.

B.1.1 Flying capacitors charge

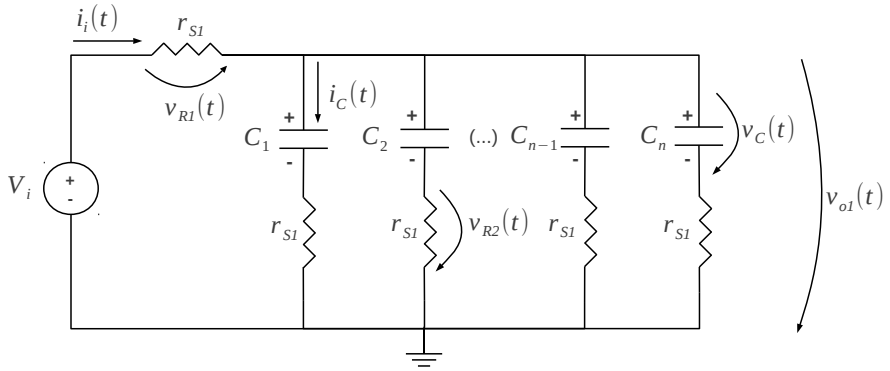

Figure B.3: Flying capacitors charge during stage 1: equivalent circuit.

Analysing figure B.3, the following equations can be drawn:

$$\begin{aligned} v_{o1}(t) &= V_i - v_{R1}(t) \\ &= V_i - r_{S1} i_i(t) \\ &= V_i - n r_{S1} C \frac{d}{dt} v_C(t) \end{aligned}$$

$$\begin{aligned} v_C(t) &= v_{o1}(t) - v_{R2}(t) \\ &= v_{o1}(t) - r_{S1} C \frac{d}{dt} v_C(t) \\ &= V_i - n r_{S1} C \frac{d}{dt} v_C(t) - r_{S1} C \frac{d}{dt} v_C(t) \\ &= V_i - (n+1) r_{S1} C \frac{d}{dt} v_C(t) \end{aligned}$$

So, in order to determine $v_C(t)$, the following differential equation has to be solved:

$$(n+1) r_{S1} C \frac{d}{dt} v_C(t) + v_C(t) = V_i \tag{B.1}$$

B.1.1.1 Solution of the differential equation

Applying the Laplace transform to equation B.1 results in:

$$\begin{aligned} &(n+1) r_{S1} C [s V_C(s) - v_C(t_0^-)] + V_C(s) = \frac{V_i}{s} \\ \Leftrightarrow &[s(n+1) r_{S1} C + 1] V_C(s) = \frac{V_i}{s} + (n+1) r_{S1} v_C(t_0^-) \\ \Leftrightarrow &V_C(s) = \left[\frac{V_i}{s} + (n+1) r_{S1} C v_C(t_0^-) \right] \frac{1}{s(n+1) r_{S1} C + 1} \\ \Leftrightarrow &V_C(s) = \left[\frac{V_i}{s} + (n+1) r_{S1} C v_C(t_0^-) \right] \frac{\frac{1}{(n+1) r_{S1} C}}{s + \frac{1}{(n+1) r_{S1} C}} \end{aligned}$$

Considering $\frac{1}{(n+1) r_{S1} C} = p_1$

$$V_C(s) = \left[\frac{V_i}{s} + \frac{1}{p_1} v_C(t_0^-) \right] \frac{p_1}{s + p_1} \tag{B.2}$$

The natural response is found by making $V_i = 0$ in equation B.2.

$$V_C^N(s) = \frac{1}{p_1} v_C(t_0^-) \frac{p_1}{s + p_1} = v_C(t_0^-) \frac{1}{s + p_1}$$

which in the time domain corresponds to

$$v_C^N(t) = v_C(t_0^-)e^{tp_1}$$

The forced response is given by making $v_C(t_0^-) = 0$ in equation B.2.

$$V_C^F(s) = V_i \frac{p_1}{s(s+p_1)} = V_i \left[\frac{A_1}{s} + \frac{A_2}{s+p_1}\right]$$

Applying the undetermined coefficient method yields:

$$A_1(s+p_1) + sA_2 = s(A_1+A_2) + p_1A_1$$

$$\begin{cases} A_1 + A_2 = 0 \\ p_1A_2 = p_1 \end{cases} \Leftrightarrow \begin{cases} A_1 = 1 \\ A_2 = -A_1 = -1 \end{cases}$$

Therefore, in the s-domain, the forced response is given by:

$$V_C^F(s) = V_i \left[\frac{1}{s} - \frac{1}{s+p_1}\right]$$

which in the time domain corresponds to

$$v_C^F(t) = V_i(1 - e^{-tp_1})$$

The complete response is given by the sum of forced and natural responses:

$$v_C(t) = v_C(t_0^-)e^{-tp_1} + V_i(1 - e^{-tp_1}) \tag{B.3}$$

for $0 \leq t < DT_s$.

B.1.2 Output discharge

Analysing the circuit from figure B.4, the following equations can be drawn:

$$i_o(t) = \frac{1}{R_L} v_o(t)$$

$$i_C L(t) = C_L \frac{d}{dt} v_o(t)$$

$$i_o(t) + i_L(t) = 0$$

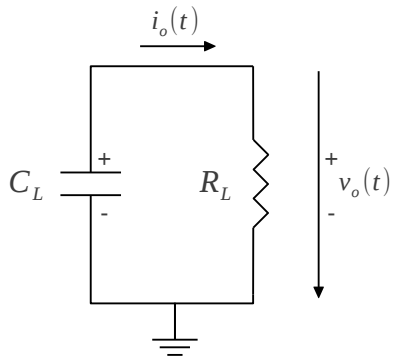

Figure B.4: Output discharge during stage 1: equivalent circuit.

which results in the following differential equation:

$$\frac{1}{R_L}v_o(t) + C_L\frac{d}{dt}v_o(t) = 0$$

B.1.2.1 Solution of the differential equation

Applying the Laplace transform to equation B.1.2:

$$\begin{aligned}
&\frac{1}{R_L}V_o(s) + C_L[sV_o(s) - v_o(t_0^-)] = 0 \\
\Leftrightarrow &\left(\frac{1}{R_L} + sC_L\right)V_o(s) = C_L v_o(t_0^-) \\
\Leftrightarrow &\left(\frac{1+sR_LC_L}{R_L}\right)V_o(s) = C_L v_o(t_0^-) \\
\Leftrightarrow &V_o(s) = v_o(t_0^-)\left(\frac{R_LC_L}{1+sR_LC_L}\right) \\
\Leftrightarrow &V_o(s) = v_o(t_0^-)\left(\frac{1}{s+\frac{1}{R_LC_L}}\right)
\end{aligned}$$

Considering $\frac{1}{R_LC_L} = p_2$, the previous equation becomes:

$$V_o(s) = v_o(t_0^-)\left(\frac{1}{s+p_2}\right) \tag{B.4}$$

which in the time domain corresponds to the following expression:

$$v_o(t) = v_o(t_0^-)e^{-tp_2} \tag{B.5}$$

for $0 \leq t \leq DT_s$

B.2 Operation during stage 2

When the $S_{2,j}$ switches are on, the circuit shown in figure B.1 becomes equivalent to the circuit in figure B.5

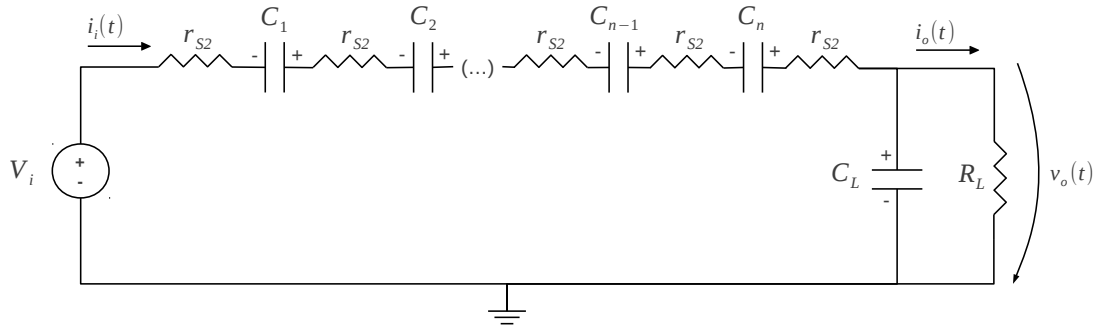

Figure B.5: Output charge during stage 2: equivalent circuit

To simplify the analysis, the series of r_s resistors is substituted with an equivalent resistor R_s

$$R_s = (n+1)r_s \tag{B.6}$$

and the series of flying capacitors is replaced with an equivalent capacitor C_{se}, where the *se* stands for *series equivalent*

$$C_{se} = \frac{C}{n} \tag{B.7}$$

The simplified circuit is shown in figure B.6.

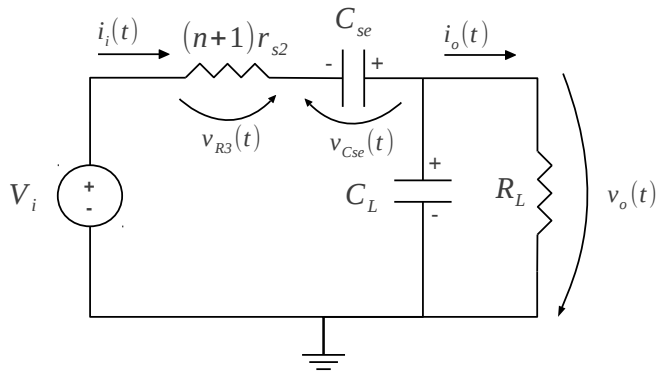

Figure B.6: Output charge during stage 2: simplified circuit.

Analysing the circuit in figure B.6, the following relationships can be drawn:

$$\begin{aligned}
& i_i(t) - i_{CL}(t) = i_o(t) \\
\Leftrightarrow & - i_{Cse}(t) - i_{CL}(t) = i_o(t) \\
\Leftrightarrow & - i_{Cse}(t) - i_{CL}(t) = i_o(t) \\
\Leftrightarrow & - C_{se}\frac{d}{dt}v_{Cse}(t) - C_L\frac{d}{dt}v_o(t) = \frac{1}{R_L}v_o(t) \\
\\
\Leftrightarrow & -C_{se}\frac{d}{dt}v_{Cse}(t) = C_L\frac{d}{dt}v_o(t) + \frac{1}{R_L}v_o(t)
\end{aligned} \tag{B.8}$$

$$\begin{aligned}
& v_o(t) = V_i - v_R3(t) + v_{Cse}(t) \\
\Leftrightarrow & v_o(t) = V_i - (n+1)r_{S2}i_i(t) + v_{Cse}(t) \\
\Leftrightarrow & v_o(t) = V_i + (n+1)r_{S2}i_{Cse}(t) + v_{Cse}(t) \\
\\
\Leftrightarrow & v_o(t) = V_i + (n+1)r_{S2}C_{se}\frac{d}{dt}v_{Cse}(t) + v_{Cse}(t)
\end{aligned} \tag{B.9}$$

Therefore, to determine $v_o(t)$ and $v_C(t)$, it is necessary to solve the following system of differential equations:

$$\begin{cases}
C_L\frac{d}{dt}v_o(t) + \frac{1}{R_L}v_o(t) = -C_{se}\frac{d}{dt}v_{Cse}(t) \\
v_o(t) = V_i + (n+1)r_{S2}C_{se}\frac{d}{dt}v_{Cse}(t) + v_{Cse}(t)
\end{cases} \tag{B.10}$$

where $v_{Cse}(t) = nv_C(t)$.

B.2.0.2 Solution of the differential equations

Applying the Laplace Transform to equation B.8 yields

$$
\begin{aligned}
&-C_{se}[sV_{Cse}(s)-v_{Cse}(t_1^-)] = C_L[sV_o(s)-v_o(t_1^-)] + \frac{1}{R_L}V_o(s)\\
\Leftrightarrow &-sC_{se}V_{Cse}(s)+C_{se}v_{Cse}(t_1^-) = sC_LV_o(s)+\frac{1}{R_L}V_o(s)-C_Lv_o(t_1^-)\\
\Leftrightarrow &-sC_{se}V_{Cse}(s) = \left(\frac{1}{R_L}+sC_L\right)V_o(s)-C_{se}v_{Cse}(t_1^-)-C_Lv_o(t_1^-)\\
\Leftrightarrow &V_{Cse}(s) = \frac{1}{sC_{se}}\left[-\left(\frac{1+sR_LC_L}{R_L}\right)V_o(s)+C_{se}v_{Cse}(t_1^-)+C_Lv_o(t_1^-)\right]\\
\Leftrightarrow &V_{Cse}(s) = -\left(\frac{1+sR_LC_L}{sR_LC_{se}}\right)V_o(s)+\frac{1}{s}v_{Cse}(t_1^-)+\frac{C_L}{sC_{se}}v_o(t_1^-)\\
\Leftrightarrow &V_{Cse}(s) = -\frac{C_L}{C_{se}}\left(\frac{s+\frac{1}{R_LC_L}}{s}\right)V_o(s)+\frac{1}{s}v_{Cse}(t_1^-)+\frac{C_L}{sC_{se}}v_o(t_1^-)
\end{aligned}
$$

Considering $G_1 = \frac{C_L}{C_{se}} = \frac{C_L}{\frac{C}{n}} = \frac{nC_L}{C}$ and $G_2 = \frac{1}{R_LC_L}$:

$$
V_{Cse}(s) = -G_1\left(\frac{s+G_2}{s}\right)V_o(s)+\frac{1}{s}v_{Cse}(t_1^-)+\frac{G_1}{s}v_o(t_1^-) \tag{B.11}
$$

Applying the Laplace Transform to equation B.9 yields

$$
\begin{aligned}
&V_o(s) = \frac{V_i}{s}+(n+1)r_{S2}C_{se}[sV_{Cse}(s)-v_{Cse}(t_1^-)]+V_{Cse}(s)\\
\Leftrightarrow &V_o(s) = \frac{V_i}{s}+s(n+1)r_{S2}C_{se}V_{Cse}(s)-(n+1)r_{S2}C_{se}v_{Cse}(t_1^-)+V_{Cse}(s)\\
\Leftrightarrow &V_o(s)-(s(n+1)r_{S2}C_{se}+1)V_{Cse}(s) = +\frac{V_i}{s}-(n+1)r_{S2}C_{se}v_{Cse}(t_1^-)
\end{aligned}
$$

Considering $G_3 = (n+1)r_{S2}C_{se} = (n+1)r_{S2}\frac{C}{n}$ the previous equation becomes

$$
V_o(s)-(sG_3+1)V_{Cse}(s) = \frac{V_i}{s}-G_3v_{Cse}(t_1^-) \tag{B.12}
$$

Substituting equation B.11 in the previous equation yields:

$$V_o(s)-(sG_3+1)\left[-G_1\left(\frac{s+G_2}{s}\right)V_o(s)+\frac{1}{s}v_{Cse}(t_1^-)+\frac{G_1}{s}v_o(t_1^-)\right]=\frac{V_i}{s}-G_3v_{Cse}(t_1^-)$$
$$\Leftrightarrow sV_o(s)-(sG_3+1)\left[-G_1(s+G_2)V_o(s)+v_{Cse}(t_1^-)+G_1v_o(t_1^-)\right]=V_i-sG_3v_{Cse}(t_1^-)$$
$$\Leftrightarrow sV_o(s)+G_1(sG_3+1)(s+G_2)V_o(s)-(sG_3+1)v_{Cse}(t_1^-)-G_1(sG_3+1)v_o(t_1^-)=V_i-sG_3v_{Cse}(t_1^-)$$
$$\Leftrightarrow[s+G_1(sG_3+1)(s+G_2)]V_o(s)=V_i-sG_3v_{Cse}(t_1^-)+(sG_3+1)v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)$$
$$\Leftrightarrow[s+s^2G_1G_3+sG_1G_2G_3+sG_1+G_1G_2]V_o(s)=V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)$$
$$\Leftrightarrow[s^2G_1G_3+s(G_1G_2G_3+G_1+1)+G_1G_2]V_o(s)=V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)$$
$$\Leftrightarrow V_o(s)=\left[V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)\right]\frac{1}{s^2G_1G_3+s(G_1G_2G_3+G_1+1)+G_1G_2}$$
$$\Leftrightarrow V_o(s)=\left[V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)\right]\frac{\frac{1}{G_1G_3}}{s^2+s\left(\frac{G_1G_2G_3+G_1+1}{G_1G_3}\right)+\frac{G_2}{G_3}}$$

Considering

$$p_{3,4}=\frac{1}{2}\left(-\frac{G_1G_2G_3+G_1+1}{G_1G_3}\pm\sqrt{\left(\frac{G_1G_2G_3+G_1+1}{G_1G_3}\right)^2-4\frac{G_2}{G_3}}\right) \tag{B.13}$$

$$V_o(s)=\left[V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)\right]\frac{\frac{1}{G_1G_3}}{(s-p_3)(s-p_4)} \tag{B.14}$$

the forced response is obtained by:

$$V_o^F(s)=\frac{\frac{1}{G_1G_3}}{(s-p_3)(s-p_4)}V_i$$
$$\Leftrightarrow V_o^F(s)=\frac{V_i}{G_1G_3}\frac{A_3}{s-p_3}+\frac{A_4}{s-p_4}$$

Using the undetermined coefficient method to determine the coefficients A_3 and A_4:

$$1=A_3(s-p_4)+A_4(s-p_3)$$
$$\Leftrightarrow 1=sA_3-A_3p_4+sA_4-A_4p_3$$
$$\Leftrightarrow 1=s(A_3+A_4)-A_3p_4-A_4p_3$$

$$\begin{cases}0 &= A_3+A_4\\ 1 &= -A_3p_4-A_4p_3\end{cases}\Leftrightarrow\qquad\begin{cases}A_3 &= \frac{1}{p_3-p_4}\\ A_4 &= -\frac{1}{p_3-p_4}\end{cases}$$

$$V_o^F(s) = \frac{\frac{1}{G_1G_3}}{p_3 - p_4}\left(\frac{1}{s-p_3} - \frac{1}{s-p_4}\right)V_i \tag{B.15}$$

which in the time domain corresponds to

$$v_o^F(t) = \frac{\frac{1}{G_1G_3}}{p_3 - p_4}\left(e^{tp_3} - e^{tp_4}\right)V_i \tag{B.16}$$

The natural response is given by:

$$\begin{aligned} V_o^N(s) &= \left[v_{Cse}(t_1^-) + G_1(sG_3+1)v_o(t_1^-)\right]\frac{\frac{1}{G_1G_3}}{(s-p_3)(s-p_4)} \\ \Leftrightarrow V_o^N(s) &= \frac{1}{G_1G_3}\frac{A_5}{s-p_3} + \frac{A_6}{s-p_4} \end{aligned}$$

Using the undetermined coefficient method to determine the coefficients A_5 and A_6:

$$\begin{aligned} &[v_{Cse}(t_1^-) + G_1(sG_3+1)v_o(t_1^-)] = A_5(s-p_4) + A_6(s-p_5) \\ \Leftrightarrow &v_{Cse}(t_1^-) + sG_1G_3v_o(t_1^-) + G_1v_o(t_1^-) = A_5s - A_5p_4 + A_6s - A_6p_5 \\ \Leftrightarrow &sG_1G_3v_o(t_1^-) + G_1v_o(t_1^-) + v_{Cse}(t_1^-) = s(A_5+A_6) - A_5p_4 - A_6p_5 \end{aligned}$$

$$\begin{cases} G_1G_3v_o(t_1^-) & = A_5 + A_6 \\ G_1v_o(t_1^-) + v_{Cse}(t_1^-) & = -A_5p_4 - A_6p_3 \end{cases} \Leftrightarrow \quad \begin{cases} A_5 & = \frac{v_{Cse}(t_1^-) + G_1(G_3p_3+1)v_o(t_1^-)}{p_3-p_4} \\ A_6 & = -\frac{v_{Cse}(t_1^-) + G_1(G_3p_4+1)v_o(t_1^-)}{p_3-p_4} \end{cases}$$

$$\begin{aligned} V_o^N(s) &= \frac{\frac{1}{G_1G_3}}{p_3-p_4}\left[\frac{v_{Cse}(t_1^-) + G_1(G_3p_3+1)v_o(t_1^-)}{s-p_3} - \frac{v_{Cse}(t_1^-) + G_1(G_3p_4+1)v_o(t_1^-)}{s-p_4}\right] \\ \Leftrightarrow V_o^N(s) &= \frac{\frac{1}{G_1G_3}}{p_3-p_4}\left[\left(\frac{1}{s-p_3} - \frac{1}{s-p_4}\right)v_{Cse}(t_1^-) + G_1\left((G_3p_3+1)\frac{1}{s-p_3} - (G_3p_4+1)\frac{1}{s-p_4}\right)v_o(t_1^-)\right] \end{aligned}$$

which in the time domain corresponds to

$$v_o^N(t) = \frac{\frac{1}{G_1G_3}}{p_3-p_4}\left[(e^{tp_3} - e^{tp_4})v_{Cse}(t_1^-) + G_1((G_3p_3+1)e^{tp_3} - (G_3p_4+1)e^{tp_4})v_o(t_1^-)\right] \tag{B.17}$$

Therefore, the complete response is the following:

$$
\begin{aligned}
& v_o(t) = v_o^F(t) + v_o^N(t) \\
\Leftrightarrow & v_o(t) = \frac{\frac{1}{G_1 G_3}}{p_3 - p_4}\left[(e^{tp_3} - e^{tp_4})V_i + (e^{tp_3} - e^{tp_4})v_{Cse}(t_1^-) + G_1((G_3p_3+1)e^{tp_3} - (G_3p_4+1)e^{tp_4})v_o(t_1^-)\right] \\
\Leftrightarrow & v_o(t) = \frac{\frac{1}{G_1 G_3}}{p_3 - p_4}\left[(e^{tp_3} - e^{tp_4})(V_i + v_{Cse}(t_1^-)) + G_1((G_3p_3+1)e^{tp_3} - (G_3p_4+1)e^{tp_4})v_o(t_1^-)\right]
\end{aligned}
$$

for $v_{Cse}(t_1^-) = nv_C(t_1^-)$ and

$$
\begin{aligned}
K_1 &= \frac{\frac{1}{G_1 G_3}}{p_3 - p_4} \\
G_1(G_3p_3+1) &= H_1 \qquad\qquad G_1(G_3p_4+1) = H_2
\end{aligned}
$$

The output voltage is given by:

$$
v_o(t) = K_1\left[(e^{tp_3} - e^{tp_4})(V_i + nv_C(t_1^-)) + (H_1e^{tp_3} - H_2e^{tp_4})v_o(t_1^-)\right] \tag{B.18}
$$

for $DT_s < t \leq T_S$.

Returning to equation B.11 and having in mind that $V_o(s)$ will be replaced with equation B.14:

$$
\begin{aligned}
& V_{Cse}(s) = -G_1\left(\frac{s+G_2}{s}\right)V_o(s) + \frac{1}{s}v_{Cse}(t_1^-) + \frac{G_1}{s}v_o(t_1^-) \\
\Leftrightarrow \quad & V_{Cse}(s) = \frac{\frac{1}{G_1 G_3}}{s(s-p_3)(s-p_4)}[-G_1^2G_3(s-p_3)(s-p_4)(s+G_2)V_o(s) \\
& \qquad\qquad + G_1G_3(s-p_3)(s-p_4)(v_{Cse}(t_1^-) + G_1v_o(t_1^-))] \\
\Leftrightarrow \quad & V_{Cse}(s) = \frac{\frac{1}{G_1 G_3}}{s(s-p_3)(s-p_4)}[-G_1^2G_3(s-p_3)(s-p_4)(s+G_2)V_o(s) \\
& \qquad\qquad + G_1G_3(s-p_3)(s-p_4)(v_{Cse}(t_1^-) + G_1v_o(t_1^-))] \\
\Leftrightarrow \quad & V_{Cse}(s) = \frac{\frac{1}{G_3}}{s(s-p_3)(s-p_4)}[-G_1G_3(s-p_3)(s-p_4)(s+G_2)V_o(s) \\
& \qquad\qquad + G_3(s-p_3)(s-p_4)(v_{Cse}(t_1^-) + G_1v_o(t_1^-))]
\end{aligned}
$$

Since the previous equation is too long, the expression inside the squared brackets will be divided in two small expressions and simplified separately:

Expression 1

$$
\begin{aligned}
&-G_1G_3(s-p_3)(s-p_4)(s+G_2)V_o(s)\\
&=-(s+G_2)\left[V_i+v_{Cse}(t_1^-)+G_1(sG_3+1)v_o(t_1^-)\right]\\
&=-[s^2G_1G_3v_o(t_1^-)+s(V_i+v_{Cse}(t_1^-)+G_1(1+G_2G_3)v_o(t_1^-))+G_2V_i+G_2v_{Cse}(t_1^-)+G_1G_2v_o(t_1^-)]
\end{aligned}
$$

Expression 2

$$
\begin{aligned}
&G_3(s-p_3)(s-p_4)[v_{Cse}(t_1^-)+G_1v_o(t_1^-)]\\
=\;&G_3[s^2-s(p_3+p_4)+p_3p_4][v_{Cse}(t_1^-)+G_1v_o(t_1^-)]\\
=\;&G_3s^2[v_{Cse}(t_1^-)+G_1v_o(t_1^-)]-G_3s(p_3+p_4)[v_{Cse}(t_1^-)+G_1v_o(t_1^-)]+G_3p_3p_4[v_{Cse}(t_1^-)+G_1v_o(t_1^-)]\\
=\;&s^2[G_3v_{Cse}(t_1^-)+G_1G_3v_o(t_1^-)]-s[G_3(p_3+p_4)v_{Cse}(t_1^-)+G_1G_3(p_3+p_4)v_o(t_1^-)]\\
&+G_3p_3p_4v_{Cse}(t_1^-)+G_1G_3p_3p_4v_o(t_1^-)
\end{aligned}
$$

Expression 1+2

$$
\begin{aligned}
&s^2(-G_1G_3v_o(t_1^-)+G_3v_{Cse}(t_1^-)+G_1G_3v_o(t_1^-))\\
&-s(V_i+v_{Cse}(t_1^-)+G_1(1+G_2G_3)v_o(t_1^-)+G_3(p_3+p_4)v_{Cse}(t_1^-)+G_1G_3(p_3+p_4)v_o(t_1^-))\\
&-G_2V_i-G_2v_{Cse}(t_1^-)-G_1G_2v_o(t_1^-)+G_3p_3p_4v_{Cse}(t_1^-)+G_1G_3p_3p_4v_o(t_1^-)\\
=\;&s^2G_3v_{Cse}(t_1^-)-s[V_i+[1+G_3(p_3+p_4)]v_{Cse}(t_1^-)+G_1[1+G_2G_3+G_3(p_3+p_4)]v_o(t_1^-)]\\
&-G_2V_i+[G_3p_3p_4-G_2]v_{Cse}(t_1^-)+G_1[G_3p_3p_4-G_2]v_o(t_1^-)
\end{aligned}
$$

The forced response is given by:

$$
V_{Cse}^F(s)=-\frac{V_i}{G_3}\frac{s+G_2}{s(s-p_3)(s-p_4)}=\frac{V_i}{G_3}\left(\frac{A_7}{s}+\frac{A_8}{s-p_3}+\frac{A_9}{s-p_4}\right)
$$

Using the undetermined coefficient method to determine the coefficients A_7, A_8 and A_14:

$$
\begin{aligned}
&A_7(s-p_3)(s-p_4)+sA_8(s-p_4)+sA_9(s-p_3)\\
=\;&A_7(s^2-s(p_3+p_4)+p_3p_4)+A_8(s^2-sp_4)+A_9(s^2-sp_3)\\
=\;&s^2(A_7+A_8+A_9)-s(A_7p_3+A_7p_4+A_8p_4+A_9p_3)+A_7p_3p_4
\end{aligned}
$$

$$
\begin{cases}
0 & =A_7+A_8+A_9\\
1 & =A_7p_3+A_7p_4+A_8p_4+A_9p_3\\
-G_2 & =A_7p_3p_4
\end{cases}
$$

$$\Leftrightarrow \begin{cases} A_7 &= -\frac{G_2}{p_3 p_4} \\ A_8 &= -\frac{G_2+p_3}{p_3(p_3-p_4)} \\ A_9 &= \frac{G_2+p_4}{p_4(p_3-p_4)} \end{cases}$$

$$V_{Cse}^F(s) = -\frac{\frac{1}{G_3}}{p_3-p_4}\left[\frac{G_2(p_3-p_4)}{p_3p_4}\frac{1}{s} + \frac{G_2+p_3}{p_3}\frac{1}{s-p_3} - \frac{G_2+p_4}{p_4}\frac{1}{s-p_4}\right]V_i$$

which in the time domain corresponds to

$$v_{Cse}^F(t) = -\frac{\frac{1}{G_3}}{p_3-p_4}\left[\frac{G_2(p_3-p_4)}{p_3p_4} + \frac{G_2+p_3}{p_3}e^{tp_3} - \frac{G_2+p_4}{p_4}e^{tp_4}\right]V_i$$

The natural response is given by:

$$V_{Cse}^N(s) = \frac{1}{G_3}\left(\frac{A_{10}}{s} + \frac{A_{11}}{s-p_3} + \frac{A_{12}}{s-p_4}\right)$$

Using the undetermined coefficient method to determine the coefficients A_{10},A_{11} and A_{12}:

$$s^2(A_{10}+A_{11}+A_{12}) - s(A_{10}p_3 + A_{10}p_4 + A_{11}p_4 + A_{12}p_3) + A_{10}p_3p_4$$

$$\begin{cases} G_3 v_{Cse}(t_1^-) & = A_{10}+A_{11}+A_{12} \\ (1+G_3(p_3+p_4))v_{Cse}(t_1^-) + G_1(1+G_2G_3+G_3(p_3+p_4)v_o(t_1^-)) & = A_{10}p_3 + A_{10}p_4 + A_{11}p_4 + A_{12}p_3 \\ (G_3p_3p_4 - G_2)v_{Cse}(t_1^-) + G_1(G_3p_3p_4 - G_2)v_o(t_1^-) & = A_{10}p_3p_4 \end{cases}$$

$$\Leftrightarrow \begin{cases} A_9 &= -\frac{1}{p_3p_4}[(G_2 - G_3p_3p_4)v_{Cse}(t_1^-) + G_1(G_2 - G_3p_3p_4)v_o(t_1^-)] \\ A_{11} &= -\frac{1}{p_3(p_3-p_4)}[(G_2+p_3)v_{Cse}(t_1^-) + G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)v_o(t_1^-)] \\ A_{12} &= \frac{1}{p_4(p_3-p_4)}[(G_2+p_4)v_{Cse}(t_1^-) + G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)v_o(t_1^-)] \end{cases}$$

$$\begin{aligned} V_{Cse}^N(s) = -\frac{\frac{1}{G_3}}{p_3-p_4}[&\frac{p_3-p_4}{p_3p_4}\frac{1}{s}[(G_2 - G_3p_3p_4)v_{Cse}(t_1^-) + G_1(G_2 - G_3p_3p_4)v_o(t_1^-)] \\ &+ \frac{1}{p_3}\frac{1}{s-p_3}[(G_2+p_3)v_{Cse}(t_1^-) + G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)v_o(t_1^-)] \\ &- \frac{1}{p_4}\frac{1}{s-p_4}[(G_2+p_4)v_{Cse}(t_1^-) + G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)v_o(t_1^-)]] \end{aligned}$$

which in the time domain corresponds to

$$\begin{aligned} v_{Cse}^{N}(t) = -\frac{\frac{1}{G_3}}{p_3-p_4}[\quad & \frac{p_3-p_4}{p_3p_4}[(G_2-G_3p_3p_4)v_{Cse}(t_1^-)+G_1(G_2-G_3p_3p_4)v_o(t_1^-)] \\ & +\frac{1}{p_3}e^{tp_3}[(G_2+p_3)v_{Cse}(t_1^-)+G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)v_o(t_1^-)] \\ & -\frac{1}{p_4}e^{tp_4}[(G_2+p_4)v_{Cse}(t_1^-)+G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)v_o(t_1^-)]] \end{aligned}$$

$$\begin{aligned} \Leftrightarrow \qquad v_{Cse}^{N}(t) = -\frac{\frac{1}{G_3}}{p_3-p_4}[& \left(\frac{p_3-p_4}{p_3p_4}(G_2-G_3p_3p_4)+\frac{1}{p_3}(G_2+p_3)e^{tp_3}-\frac{1}{p_4}(G_2+p_4)e^{tp_4}\right)v_{Cse}(t_1^-)+ \\ & \left(\frac{p_3-p_4}{p_3p_4}+\frac{1}{p_3}G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)e^{tp_3}-\frac{1}{p_4}G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)e^{tp_4}\right)v_o(t_1^-)] \end{aligned}$$

Therefore, the complete response is the following:

$$\begin{aligned} & v_{Cse}(t) = v_{Cse}^{F}(t)+v_{Cse}^{N}(t) \\ \Leftrightarrow & v_{Cse}(t) = -\frac{\frac{1}{G_3}}{p_3-p_4}[\\ & \left(\frac{G_2(p_3-p_4)}{p_3p_4}+\frac{G_2+p_3}{p_3}e^{tp_3}-\frac{G_2+p_4}{p_4}e^{tp_4}\right)V_i \\ & +\left(\frac{p_3-p_4}{p_3p_4}(G_2-G_3p_3p_4)+\frac{1}{p_3}(G_2+p_3)e^{tp_3}-\frac{1}{p_4}(G_2+p_4)e^{tp_4}\right)v_{Cse}(t_1^-) \\ & +\left(\frac{p_3-p_4}{p_3p_4}+\frac{1}{p_3}G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)e^{tp_3}-\frac{1}{p_4}G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)e^{tp_4}\right)v_o(t_1^-)] \end{aligned}$$

The voltage drop of each capacitor during stage 2 is then given by:

$$\begin{aligned} & v_C(t) = \frac{1}{n}v_{Cse}(t) \\ \Leftrightarrow & v_C(t) = -\frac{\frac{1}{G_3}}{n(p_3-p_4)}[\\ & \left(\frac{G_2(p_3-p_4)}{p_3p_4}+\frac{G_2+p_3}{p_3}e^{tp_3}-\frac{G_2+p_4}{p_4}e^{tp_4}\right)V_i \\ & +\left(\frac{p_3-p_4}{p_3p_4}(G_2-G_3p_3p_4)+\frac{1}{p_3}(G_2+p_3)e^{tp_3}-\frac{1}{p_4}(G_2+p_4)e^{tp_4}\right)nv_C(t_1^-) \\ & +\left(\frac{p_3-p_4}{p_3p_4}+\frac{1}{p_3}G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3)e^{tp_3}-\frac{1}{p_4}G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4)e^{tp_4}\right)v_o(t_1^-)] \end{aligned} \tag{B.19}$$

Considering:

$$\frac{\frac{1}{G_3}}{n(p_3-p_4)} = K_2$$

$$\frac{p_3-p_4}{p_3p_4}(G_3p_3p_4) = M_1 \qquad \frac{G_2+p_4}{p_4} = M_4 \qquad \frac{1}{p_3}G_1(G_2+p_3+G_3p_3^2+G_2G_3p_3) = M_6$$

$$\frac{p_3-p_4}{p_3p_4}G_2 = M_2 \qquad \frac{p_3-p_4}{p_3p_4} = M_5 \qquad \frac{1}{p_4}G_1(G_2+p_4+G_3p_4^2+G_2G_3p_4) = M_7$$

$$\frac{G_2+p_3}{p_3} = M_3$$

the previous equation becomes

$$\begin{aligned} v_C(t) = K_2[M_1 n v_C(t_1^-) - (M_2 + M_3 e^{tp_3} - M_4 e^{tp_4})(V_i + n v_C(t_1^-)) \\ - (M_5 + M_6 e^{tp_3} - M_7 e^{tp_4}) v_o(t_1^-)] \end{aligned} \tag{B.20}$$

$0 \leq t < (1-D)T_s$

B.3 Summary

During stage 1:

$$\begin{aligned} v_o(t) &= v_o(t_0^-)e^{-tp_2} \\ v_C(t) &= v_C(t_0^-)e^{-tp_1} + V_i(1-e^{-tp_1}) \end{aligned}$$

for $0 \leq t < DT_s$.

During stage 2:

$$\begin{aligned} v_o(t) =& K_1\left[(e^{tp_3}-e^{tp_4})(V_i+nv_C(t_1^-)) + (H_1e^{tp_3}-H_2e^{tp_4})v_o(t_1^-)\right] \\ v_C(t) =& K_2[M_1nv_C(t_1^-) - (M_2+M_3e^{tp_3}-M_4e^{tp_4})(V_i+nv_C(t_1^-)) - (M_5+M_6e^{tp_3}-M_7e^{tp_4})v_o(t_1^-)] \end{aligned}$$

for $0 \leq t < (1-D)T_s$.

where

$$G_1 = \frac{nC_L}{C} \qquad K_1 = \frac{\frac{1}{G_1G_3}}{p_3-p_4}$$

$$G_2 = \frac{1}{R_LC_L} \qquad K_2 = \frac{\frac{1}{G_1}}{n(p_3-p_4)}$$

$$G_3 = \frac{(n+1)}{n}r_{S2}C$$

$$H_1 = G_1(G_3 p_3 + 1)$$
$$H_2 = G_1(G_3 p_4 + 1)$$

$$M_1 = G_3(p_3 - p_4) \qquad M_5 = \frac{p_3 - p_4}{p_3 p_4}$$
$$M_2 = \frac{p_3 - p_4}{p_3 p_4} G_2 \qquad M_6 = \frac{1}{p_3} G_1(G_2 + p_3 + G_3 p_3^2 + G_2 G_3 p_3)$$
$$M_3 = \frac{G_2 + p_3}{p_3} \qquad M_7 = \frac{1}{p_4} G_1(G_2 + p_4 + G_3 p_4^2 + G_2 G_3 p_4)$$
$$M_4 = \frac{G_2 + p_4}{p_4}$$

$$p_1 = \frac{1}{(n+1) r_{S1} C} \qquad p_2 = \frac{1}{R_L C_L}$$

$$p_{3,4} = \frac{1}{2}\left(-\frac{G_1 G_2 G_3 + G_1 + 1}{G_1 G_3} \pm \sqrt{\left(\frac{G_1 G_2 G_3 + G_1 + 1}{G_1 G_3} \right)^2 - 4\frac{G_2}{G_3}} \right)$$

Appendix C

Source Code

The computational calculations were all performed with the open source software Scilab. The main source code developed is shown in the present appendix.

C.1 functionLibrary.sci

```
0001 //NOTE: After the Scilab startup, run this file once to load the functions into
0002 //      the workspace.
0003
0004 function [Ao]=SquareWaveGenerator(f, D, t, tsp)
0005 //Function description: Constant square wave generator with a minimum amplitude
0006 //of 0 and a maximum amplitude of 1. During each period begins with an
0007 //amplitude of 1 and remains with it during D*T. Then is set to zero until the
0008 //period is over. To obtain an inverse wave, which during each period begins
0009 //with an amplitude of 0 and them is set to 1 when the D*T time period is over:
0010 //abs(SquareWaveGenerator(fs, D, ta, tsp)-1).
0011 //Input arguments
0012 // f: Square wave frequency (Hz)
0013 // D: Duty-cycle (%)
0014 // t: Total time (s)
0015 // tsp: time step (s)
0016 //Output arguments
0017 // Ao: vector with the same length of t which represents the amplitude of the
0018 //square wave and has the values 0 or 1.
0019
0020 T = 1/f;          // Wave period
0021 D = D/100;        // The duty-cycle is given in %. Passage to [0;1] range
0022 Ao=0;            // Output initialization
0023
0024 // Auxiliary variables initialization
0025 i=1; j=1; k=0;
0026 counter=0;       // Represents the number of samples during one period
0027 Aaux=0;          // Is assigned with the values 1 and 0 during one period
0028
0029
0030 // During stage 1 ([0;DT[) the square wave amplitude is set to 1
0031 for i=0:tsp:T*D-tsp
0032    counter = counter + 1;
0033    Aaux(counter) = 1;
0034 end
0035
0036 // During stage 2 ([DT;T[) the square wave amplitude is set to 0
0037 for i=T*D:tsp:T-tsp
0038    counter = counter + 1;
0039    Aaux(counter) = 0;
0040 end
0041
0042 // During each period, the vector Ao is assigned with the values of the
0043 //auxiliary variable Aaux until t is over
0044 for j=1:length(t)
0045    k=k+1;
0046    Ao(j) = Aaux(k);
0047
0048    // When k = counter means that one period is over and another will start, so
0049    //the vector Aaux will have to be read from the beginning. Thus, k has to
0050    //be set to 0.
0051    if k == counter then k=0; end
0052 end
0053
0054 endfunction
0055
0056 function [vo, vC, to]=SystemModel(fs, D1, D2, m, Vi, n, C, rs1, rs2, CL, RL, voi, vCi)
0057 // Function Description: Given a set of parameters, computes the output and
0058 //flying capacitors voltage of a step-up swiched capacitor DC-DC converter with
0059 //a series-parallel topology with a theoretical voltage ratio of n+1. In every
0060 //cycle the converter has two (sometimes 3) operation stages:
0061 // Stage 1: The n flying capacitors charge in parallel with the source, and the
0062 //output is disconnected from the input.
```

```
0063 // Stage 2: The flying capacitors discharge in series with the source charging
0064 //the output.
0065 // Middle Stage: May occur between stage 1 and 2. The flying capacitors are no
0066 //longer charging, and are disconnected from both input and output. Their
0067 //voltage remains constant. However the output remains disconnected form the
0068 //source, so it keeps discharging.
0069 //Input parameters
0070 // fs: Switching frequency (Hz)
0071 // D1: Duty-cycle of phi1 (%)
0072 // D2: Duty-cycle of phi2 (%)
0073 // m: Number of operation cycles
0074 // Vi: Input voltage (V)
0075 // n: Number of flying capacitors
0076 // C: Flying capacitors (F)
0077 // rs1: Switch on-resistance during stage 1 (ohm)
0078 // rs2: Switch on-resistance during stage 2 (ohm)
0079 // CL: Load Capacitor (F)
0080 // RL: Load Resistor (Ohm)
0081 // voi: Initial output voltage (V)
0082 // vCi :Initial voltage per flying capacitor (V)
0083 //Output parameter
0084 // vo: Output voltage (V)
0085 // vC: Voltage per flying capacitor (V)
0086 // to: Total operation time (s)
0087
0088 // Model definitions
0089 Ts=1/fs;                    //Switching period (s)
0090 tsp = 0.01*Ts;              //Time step (for signal sampling) (s)
0091 to = 0:tsp:m*(Ts);          //Operation time vector
0092 tr=0:tsp:Ts-tsp;            //Relative time vector
0093
0094 phi1 = SquareWaveGenerator(fs, D1, to, tsp);             //Phi1 command signal
0095 phi2 = abs(SquareWaveGenerator(fs, (100-D2), to, tsp)-1); //Phi2 command signal
0096
0097 i=0; h=0;         // Auxiliary variables
0098 vo = 0;           // Ouput voltage vetor initialization
0099 vC = 0;           // Ouput flying capaciotor voltage  initialization
0100
0101 // During stage 1 ...
0102 p1 = 1/((n+1)*rs1*C);
0103 p2 = 1/(RL*CL);
0104
0105 // During stage 2 ...
0106 G1 = n*CL/C;
0107 G2 = 1/(RL*CL);
0108 G3 = (n+1)*rs2*C/n;
0109
0110 // Coefficients of the denominator's polynomial
0111 a = 1;
0112 b = (G1*G2*G3+G1+1)/(G1*G3);
0113 c = G2/G3;
0114
0115 // Poles (zeros of the denominator's polynomial)
0116 p3 = (-b+sqrt(b^2-4*c*a))/(2*a);
0117 p4 = (-b-sqrt(b^2-4*c*a))/(2*a);
0118
0119 // Coefficients of the vo(t) function
0120 K1 = (1/(G1*G3))/(p3-p4);
0121 H1 = G1*(G3*p3+1);
0122 H2 = G1*(G3*p4+1);
0123
0124 // Coefficients of the vC(t) function
```

```
K2 = (1/G3)/(n*(p3-p4));
M1 = (p3-p4)/(p3*p4)*(G3*p3*p4);
M2 = (p3-p4)/(p3*p4)*G2;
M3 = (G2+p3)/p3;
M4 = (G2+p4)/p4;
M5 = (p3 - p4)/(p3*p4);
M6 = 1/p3*G1*(G2 + p3 + G3*p3^2 + G2*G3*p3);
M7 = 1/p4*G1*(G2 + p4 + G3*p4^2 + G2*G3*p4);

for i=1:length(to)-1

    h=h+1;

   if (phi1(i) == 1) & (phi2(i) == 0) then    // Stage 1
        //Output voltage
        vo(i)=voi*exp(-tr(h)*p2);

        //Flying capacitors voltage
        vC(i)= vCi*exp(-tr(h)*p1)+Vi*(1-exp(-tr(h)*p1));
    end

    if (phi1(i) == 0) & (phi2(i) == 0) then    // Middle Stage
        //Output voltage
        vo(i)=voi*exp(-tr(h)*p2);

        //Flying capacitors voltage
        vC(i)= vCi;
    end

    if (phi2(i) == 1) & (phi1(i) == 0) then    // Stage 2

        //Output voltage
        vo1(i)=(exp(tr(h)*p3)-exp(tr(h)*p4))*(Vi+n*vCi);
        vo2(i)=(H1*exp(tr(h)*p3)-H2*exp(tr(h)*p4))*voi;

        vo(i)= K1*(vo1(i)+vo2(i));

        //Flying capacitors voltage
        vC1(i)=  M1*n*vCi;
        vC2(i)= -(M2+M3*exp(tr(h)*p3)-M4*exp(tr(h)*p4))*(Vi+n*vCi);
        vC3(i)= -(M5+M6*exp(tr(h)*p3)-M7*exp(tr(h)*p4))*voi;

        vC(i) = K2*(vC1(i)+vC2(i)+vC3(i));
    end

    //Phi1 falling edge detection (End of stage 1)
    if (phi1(i) == 1) & (phi1(i+1) == 0) then
        vCi=vC(i);    // update the flyng capacitors voltage initial value
    end

    //Phi2 rising edge detection (stage 2 will begin in the next cycle)
    if (phi2(i) == 0) & (phi2(i+1) == 1) then
        voi=vo(i);   // update the output voltage initial value
        h = 0;       // A switch commutation occurs, therefore, the relative time
                     //must be set to zero.
    end

    //Phi1 rising and phi2 falling edge detection
    //(End of stage 2. Stage 1 will begin in the next cycle)
    if
 ((phi1(i) == 0) & (phi1(i+1) == 1)) | ((phi2(i) == 1) & (phi2(i+1) == 0)) then
        voi=vo(i);   // update the output voltage initial value
```

```
0186          vCi=vC(i);   // update the flying capacitors voltage initial value
0187          h = 0;       // A switch commutation occurs, therefore, the relative time
0188                       //must be set to zero.
0189      end
0190
0191  end
0192
0193  //Adjustment of the vC and vo vectors to match the length of the to vector
0194  vC(i+1)=vC(i);
0195  vo(i+1)=vo(i);
0196
0197  endfunction
```

C.2 parameterExtraction.sce

```
0001  // Model parameters
0002  fs = 10e6;            // Switching frequency (Hz)
0003  D1 = 70;              // Duty-cycle of phi1 (%)
0004  D2 = 30;              // Duty-cycle of phi2 (%)
0005  m1 = 50;              // Number of operation cycles
0006
0007  Vi = 0.9;             // Input voltage (V)
0008  n = 3;                // Number of flying capacitors
0009
0010  VoRef = 2.5;          // Reference output voltage (V)
0011  IoRef =100e-3;        // Reference output current (A)
0012  VoRipple = 0.01*2.5;  // Desired voltage ripple
0013
0014  C   = 65e-9:1e-9:70e-9;     // Flying capacitors (F)
0015  rs1 = 0.2:0.05:0.4;         // Switch on-resistance during stage 1 (ohm)
0016  rs2 = 0.2:0.05:0.4;         // Switch on-resistance during stage 2 (ohm)
0017  CL  = 150e-9:1e-9:200e-9;   // Load Capacitor (F)
0018
0019  // Auxiliar initializations
0020  RL = VoRef/IoRef ;    // Load Resistor (Ohm)
0021  CL0 = 500e-9;         // Load Capacitor initial value (F)
0022  voi=VoRef;            // Initial output voltage (V)
0023  vCi=0.5*Vi;           // Initial voltage per flying capacitor (V)
0024  voLowestMean=5;
0025  C_best   = 0;
0026  rs1_best = 0;
0027  rs2_best = 0;
0028  CL_best  = 0;
0029
0030  // Main Program
0031  disp('Computing ...')
0032
0033  i=0;j=0;k=0;
0034
0035  for i=1:length(C)
0036      for j=1:length(rs1)
0037          for k=1:length(rs2)
0038
  [vo1, vC1, to1]=SystemModel(fs, D1, D2, m1, Vi, n, C(i), rs1(j), rs2(k), CL0, RL, voi, vCi);
0039
0040              index2=length(vo1);
0041              index1=round(index2-index2/3);
0042              vo1Mean=mean(vo1(index1:index2));    // Mean output voltage calculation
0043
0044              if   vo1Mean>VoRef & vo1(index1)<vo1(index2) & vo1Mean<voLowestMean then
0045                  voLowestMean=vo1Mean;
0046                  C_best=C(i);
0047                  rs1_best=rs1(j);
0048                  rs2_best=rs2(k);
0049              end
0050          end
0051      end
0052  end
0053
0054  if C_best == 0 | rs1_best == 0 | rs1_best == 0 then
0055         disp('No results found for C, rs1 and rs2 in the established intervals.')
0056  else
0057      check = 0;    //Stored capacitor flag
0058      for l=1:length(CL)
0059
  [vo2, vC2, to2]=SystemModel(fs, D1, D2, m1, Vi, n, C_best, rs1_best, rs2_best, CL(l), RL, voi, 
0060          index2=length(vo2);
```

```
0061          index1=round(index2-index2/3);
0062          vo2Max=max(vo2(index1:index2));
0063          vo2Min=min(vo2(index1:index2));
0064          vo2Ripple=(vo2Max-vo2Min)/2;        //Output voltage ripple calculation
0065
0066          if vo2Ripple < VoRipple & check ~= 1 then
0067             check = 1;
0068             CL_best = CL(l);
0069          end
0070      end
0071
0072      if CL_best == 0 then
0073         disp('No results found for CL in the established interval.')
0074      else
0075          mprintf('C_best= %f nF\n',     C_best/(1e-9));
0076          mprintf('rs1_best= %f ohm\n',      rs1_best);
0077          mprintf('rs2_best= %f ohm\n',      rs2_best);
0078          mprintf('CL_best= %f nF\n',    CL_best/(1e-9));
0079      end
0080  end
```

C.3 MOSFETdesign.sce

```
0001 //CMOS 0.35 um process parameters (Appendix A.6)
0002 L   =   0.35e-6;
0003 W   =  [1000, 2000, 3000, 4000, 5000, 6000, 7000, 8000, 9000, 10000]*10^(-6);
0004 kn  =  [34.5, 52.0, 66.5, 73.0, 79.0, 82.0, 85.5, 88.0, 90.5, 93.0 ]*10^(-6);
0005 VTn =  [0.05, 0.27, 0.42, 0.46, 0.49, 0.50, 0.51, 0.52, 0.53, 0.54 ];
0006 kp  =  [10.0, 16.5, 20.5, 23.0, 26.0, 26.5, 27.5, 28.5, 29.5, 30.0 ]*10^(-6);
0007 VTp = -[0.32, 0.35, 0.44, 0.50, 0.58, 0.58, 0.60, 0.62, 0.63, 0.64 ];
0008
0009 //MOSFETs desired on-resistance
0010 rs1 = 0.3;
0011 rs2 = 0.3;
0012
0013 //Clock voltages
0014 VH_CLK = 3;
0015 VL_CLK = 0;
0016
0017 //Input voltages
0018 ViMax = 1.5;
0019 ViMin = 0.9;
0020
0021 N = length(W);
0022 Wmax = W(N);
0023
0024 //Function that computes the length (Wi) and number of parallel MOSFETs (ni)
0025 //necessary to ensure a given equivalent on-resistance for a certain VGS,
0026 //ki, VTi and L values
0027 //Essentially, if the first computed W is superior to Wmax, a new transistor
0028 //in parallel is added and the on-resistance per/MOSFET is increased. This
0029 //process is repeated until W < Wmax.
0030 function [Wi, ni]=MOSLengthAndNumber(VGS, Ron, ki, VTi, L)
0031     ni=1;
0032     for ni=1:1:100
0033         Ron = Ron*ni;
0034         B = 1/(Ron*(abs(VGS)-abs(VTi)));
0035         Wi = (B*L)/ki;
0036         if (Wi <= Wmax) then break; end
0037     end
0038 endfunction
0039
0040 //Function that computes the error between the length computed  by function
0041 //MOSLengthAndNumber() and the length corresponding to the ki-VTi pair used.
0042 function [Werror]=errorCalculation(Wref, Wactual)
0043     Werror = (Wref - Wactual)/Wref*100;
0044 endfunction
0045
0046 //Function that returns the final length and number of MOSFETs. It receives
0047 // the process parameters as vectors and the desired equivalent on-resistance
0048 // and gate-source voltage. Computes and successively stores the W and n
0049 // values which have the smallest error.
0050 function [Wf, nf, f]=MOSdesign(VGS, Ron, k, VT, L)
0051     SmallestWerror = 100;
0052     for i=1:1:N
0053       [Wi, ni] = MOSLengthAndNumber(VGS, Ron, k(i), VT(i),L);
0054       Werror = errorCalculation(W(i), Wi);
0055
0056       if Werror < SmallestWerror & Werror > 0 then
0057           Wf = Wi;
0058           nf = ni;
0059           f=i;
0060           SmallestWerror = Werror;
0061       end
0062     end
```

```
0063  endfunction
0064
0065  //Results
0066  disp('Stage 1')
0067
0068      //S11N
0069      VGS_S11N = VH_CLK - ViMax;
0070      [W_S11N, n_S11N, f] = MOSdesign(VGS_S11N, rs1, kn, VTn);
0071
0072      mprintf('\nS11N\n');
0073      mprintf('number = %d\n', n_S11N);
0074      mprintf('W= %f um\n', W_S11N/(1e-6));
0075      mprintf('theoretical W= %f um\n', W(f)/(1e-6));
0076
0077      //S12N and S14N
0078      VGS_S12N = VH_CLK - ViMax;
0079      [W_S12N, n_S12N, f_S12N] = MOSdesign(VGS_S12N, rs1/2, kn, VTn);
0080
0081      mprintf('\nS12N and S14N\n');
0082      mprintf('number = %d\n', n_S12N);
0083      mprintf('W= %f um\n', W_S12N/(1e-6));
0084      mprintf('theoretical W= %f um\n', W(f_S12N)/(1e-6));
0085
0086      //S13N and S15N
0087      VGS_S13N = VH_CLK;
0088      [W_S13N, n_S13N, f_S13N] = MOSdesign(VGS_S13N, rs1/2, kn, VTn);
0089
0090      mprintf('\nS13N and S15N\n');
0091      mprintf('number = %d\n', n_S13N);
0092      mprintf('W= %f um\n', W_S13N/(1e-6));
0093      mprintf('theoretical W= %f um\n', W(f_S13N)/(1e-6));
0094
0095      //S16N
0096      VGS_S16N = VH_CLK;
0097      [W_S16N, n_S16N, f_S16N] = MOSdesign(VGS_S16N, rs1, kn, VTn);
0098
0099      mprintf('\nS16N\n');
0100      mprintf('number = %d\n', n_S16N);
0101      mprintf('W= %f um\n', W_S16N/(1e-6));
0102      mprintf('theoretical W= %f um\n', W(f_S16N)/(1e-6));
0103
0104  //DISCHARGE
0105  disp('Stage 2')
0106
0107      //S21N
0108      VGS_S21N = VH_CLK - ViMax;
0109      [W_S21N, n_S21N, f_S21N] = MOSdesign(VGS_S21N, rs2, kn, VTn);
0110
0111      mprintf('\nS21N\n');
0112      mprintf('number = %d\n', n_S21N);
0113      mprintf('W= %f um\n', W_S21N/(1e-6));
0114      mprintf('theoretical W= %f um\n', W(f_S21N)/(1e-6));
0115
0116
0117      //S22P, S23P and S24P
0118      VGS_S22P = VL_CLK - ViMin;
0119      [W_S22P, n_S22P, f_S22P] = MOSdesign(VGS_S22P, rs2, kp, VTp);
0120
0121      mprintf('\nS22P, S23P and S24P\n');
0122      mprintf('number = %d\n', n_S22P);
0123      mprintf('W= %f um\n', W_S22P/(1e-6));
0124      mprintf('theoretical W= %f um\n', W(f_S22P)/(1e-6));
```

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